UHF Energy Harvesting and Power Management

by

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Abstract

As we are entering the era of Internet of Things (i.e. IoT), the physical devices become increasingly connected with each other than ever before. The connection between devices is achieved through wireless communication schemes, which unfortunately consume a significant amount of energy. This is undesirable for devices which are not directly connected to power. This is because these devices will essentially carry batteries to supply the needed energy for these operations and the batteries will eventually be depleted. This motivates the need to operate these devices off harvested energy.

UHF energy harvesting, as an enabling technology for the UHF RFID, stands out amongst other energy harvesting approaches as it does not heavily rely on the natural surrounding environment and also offers a very good wireless operating range from its radiating energy source. Unlike the RFID, the power consumption and the operational range requirement of these IoT devices can vary significantly. Thus, the design of the RF energy harvesting front-end and the power management need to be re-thought for specific applications.

To that end, in this thesis, discussions mainly evolve around the design of UHF energy harvesters and their associated power management units using lower power analog approaches. First, we present the background of the low power UHF energy harvesting, specially threshold-compensated rectifiers will be presented as a key technology in this area and this will be used as a build practical harvester for the UHF RFID application. Secondly, key issues with the threshold compensation will be identified and this is exploited either (i) to improve the dynamic power conversion efficiency of the harvester, (ii) to improve dynamic settling behaviour of the harvester. To exploit the ”left-over” harvested energy, an intelligent integrated power management solution has been proposed. Finally, the charge-burst approach is exploited to implement an energy harvester with -40 dBm input power sensitivity.

HDR Thesis Declaration

I certify that this work contains no material which has been accepted for the award of any other degree or diploma in my name, in any university or other tertiary institution and, to the best of my knowledge and belief, contains no material previously published or written by another person, except where due reference has been made in the text. In addition, I certify that no part of this work will, in the future, be used in a submission in my name, for any other degree or diploma in any university or other tertiary institution without the prior approval of the University of Adelaide and where applicable, any partner institution responsible for the joint-award of this degree.

I give permission for the digital version of my thesis to be made available on the web, via the University's digital research repository, the Library Search and also through web search engines, unless permission has been granted by the University to restrict access for a period of time.

I acknowledge the support I have received for my research through the provision of an Australian Government Research Training Program Scholarship.

	18/Mar/2019
Signed	Date

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The last three years is filled with plenty of excitement for me. Living in a new city and starting a research degree, having my first paper published, and now starting a new job. I consider these to be the most valuable experiences in my life. And these would not have been possible for the people whom I would like to thank in the following.

First, I thank my principal supervisor Dr. Said Al-Sarawi for supporting my scholarship application to pursue a PhD degree at the University of Adelaide, I thank him for putting up with my, well, everything. I also thank him for his relentless financial support so that I could travel all these conferences and workshops to learn the art of UHF Energy Harvesting. Apart from the academic life, he has helped me in so many other different ways that I don't even know how to thank him.

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Thesis Conventions

The following conventions have been adopted in this Thesis:

Typesetting

This document was compiled using LaTeX2e. TeXnicCenter was used as text editor interfaced to LaTeX2e. Adobe Illustrator CS2 was used to produce schematic diagrams and other drawings.

Spelling

Australian English spelling conventions have been used, as defined in the Macquarie English Dictionary—A. Delbridge (Ed.), Macquarie Library, North Ryde, NSW, Australia, 2001.

Referencing

The Harvard reference style is used for referencing and citation in this thesis.

System of Units

The units comply with the international system of units recommended in an Australian Standard: AS ISO 1000-1998 (Standards Australia Committee ME/71, Quantities, Units and Conversions 1998).

Acronyms

AC	Alternating Current
DC	Direct Current
EM	Electromagnetic
RF	Radio Frequency
IoT	Internet of Things
IC	Integrated Circuit
CMOS	Complementary Metal Oxide Semiconductor
PCE	Power Conversion Efficiency
IFE	Interface Efficiency
EEE	End-to-end Efficiency
HPMU	Hybrid Power Management Unit
EEMU	Excess Energy Management Unit
PRU	Power Routing Unit
PMU	Power Management Unit
SoC	System on Chip
PSS	Periodic Steady State
HB	Harmonic Balance
ULP	Ultra Low Power
HF	High Frequency
UHF	Ultra High Frequency
WSN	Wireless Sensor Node

Awards and Scholarships

2014

- Australian Postgraduate Award

Publications

Journal Articles

[1] **M. Sun**, S. F. Al-Sarawi, P. Ashenden, M. Cavaiuolo, and D. C. Ranasinghe, "A Fully Integrated Hybrid Power Management Unit for Passive UHF RFID in 130-nm Process," *IEEE Journal of RFID*, vol. 1, no. 1, 2017.

Conference Articles

[1] **M. Sun**, D. Ranasinghe and S. F. Al-Sarawi, "RF energy harvester with peak power conversion efficiency tracking," in *Proc. IEEE Asia Pacific Conf. Circuits and Systems*, Jeju, South Korea, November, 2016, pp. 107–110.

[2] **M. Sun**, S. F. Al-Sarawi, P. Ashenden, M. Cavaiuolo and D. C. Ranasinghe, "A fully integrable hybrid power management unit for passive UHF RFID," in *Proc. IEEE Conference on RFID*, Phoenix, Arizona, May, 2017, pp. 198–204.

[3] **M. Sun**, D. Abbott and S. F. Al-Sarawi, "A fully integrable RF energy harvester with dynamic efficiency tuning," in *Proc. IEEE International Conference on SoC Design*, Seoul, Korea, November, 2017, pp. 61–62.

Note: Chapter 4 is loosely based on Conference [**1**], Chapter 5 is loosely based on Conference [**3**] and Chapter 6 is loosely based on Conference [**2**] and Journal [**1**].

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Chapter 1

Introduction

In the context of low-power UHF energy harvesting, both the RF energy harvesting front-end and power management units are important to wireless powered systems. In this chapter, the key challenges for both of these areas are presented, from which the contributions of this thesis are highlighted. Finally, the structure of this thesis is introduced.

1.1 A Glance at UHF Energy Harvesting

The idea of energy harvesting perhaps first originated from electricity generation, where the naturally available energy is converted to electricity in a centrally-controlled power plant and then distributed to households and factories. Contrary to electricity generation, the electrical power generated by an energy harvester is of much lower level and is typically consumed locally. The target applications of energy harvesting are mostly low-power or ultra-low-power electronic devices such as wireless sensors and RFID tags. The most obvious advantage of these devices is that they do not require power cords or batteries, which are mandated by traditional electronic devices.

There are many different types of energy harvesting, namely solar, kinetic, thermoelectric and RF energy harvesting. Solar energy harvesting exploits photovoltaic cells to convert solar energy into electrical energy. Its conversion efficiency is limited and availability of the solar energy also depends upon the surrounding environment of the energy harvester (Alippi et al., 2008; Brunelli et al., 2009). For thermoelectric energy harvesting, one of the main applications is the detection of hot surface, where the temperature gradient is used to generate electrical energy and this energy can be subsequently used by sensors to measure the temperature and send the data wirelessly back to the base station (Sodano et al., 2007). Kinetic energy harvesting is typically used in wearable sensors, where human motion can be used to generate electrical energy, which can then be used to collect human vital information such as heart beat and body temperature (Roundy et al., 2003). The aforementioned approaches such as solar, kinetic and thermoelectric energy harvesting schemes are typically designed to harvest energy from unintentional energy sources and they are dependent upon the availability of energy resources (solar, kinetic and thermal) which is random in nature. RF energy harvesting, on the other hand, is typically designed to harvest from intentionally emitting energy sources, which can be better regulated and controlled. Another advantage of the RF energy harvester is that it is normally more cost-effective than the other types of energy harvesters. The fundamental reason is that energy conversion units of other energy harvesters are often not compatible with the low-cost baseline CMOS process whereas the RF energy harvesters can be easily integrated and can share the same antenna with wireless sensor (Papotto et al., 2018).

Within RF energy harvesting, there are mainly two different types. The first type is based on high frequency (i.e. HF) (13.56 MHz) standards that is widely employed in

day-to-day commercial products. Traditional examples include smart card (ID card, transportation card, and etc) and more recent examples include wireless charging of mobile phones. These energy harvesting devices typically harvest the near field EM energy at 13.56 MHz. The other type of energy harvester operates at ultra-high-frequency (i.e. UHF) and it harvests the far field EM energy. In contrast to its HF counterpart, the operational range of the UHF harvester is substantially longer while its harvested power is typically lower. With the advent of low power and ultra-low-power circuit systems, which have been designed to operate under uW, nW and sometimes even pW power levels (Seok et al., 2008). The energy harvested in UHF domain is more than sufficient to provide the needed power for these circuitry.

The design of low power energy harvester, however, poses several challenges. Firstly, as the input power decreases, the input amplitude drops substantially, the rectifying devices within the harvester enter into sub-threshold region. When the devices are in sub-threshold, the output current of these devices are tiny, resulting in very poor PCE. Thus, new rectifier circuit topologies are needed to move rectifying devices out of the sub-threshold regions as much as possible.

Another challenge for the design of UHF harvester is the need to understand the power conversion efficiency. This efficiency consists of mainly two parts: the rectifier-antenna (or, whatever the power source is used) interface efficiency, as well as, the intrinsic power conversion efficiency of the rectifier circuit. The input impedance of rectifier without an interfacing power source is meaningless, because it is defined by interactions between the source impedance and rectifier input impedance. The load of the rectifier also plays a significant role on the overall harvesting efficiency. For example, when the load increases, the output voltage and current of the rectifier will change, and the input impedance of the rectifier (the interface efficiency) will change, then the input power absorbed by the rectifier will change, then the PCE of the rectifier will change. As can be understood, the overall efficiency (even for the steady state) of the UHF harvester is a complex, non-linear, interdependent process of many different factors/components within the system.

To improve the performance of the rectifier, quite often, auxiliary rectifiers or auxiliary circuits need to be introduced as part of the system for faster start-up and better conversion efficiency in the steady state. An additional challenge is that the final harvested power is very low due to the low level of the input power, as such these

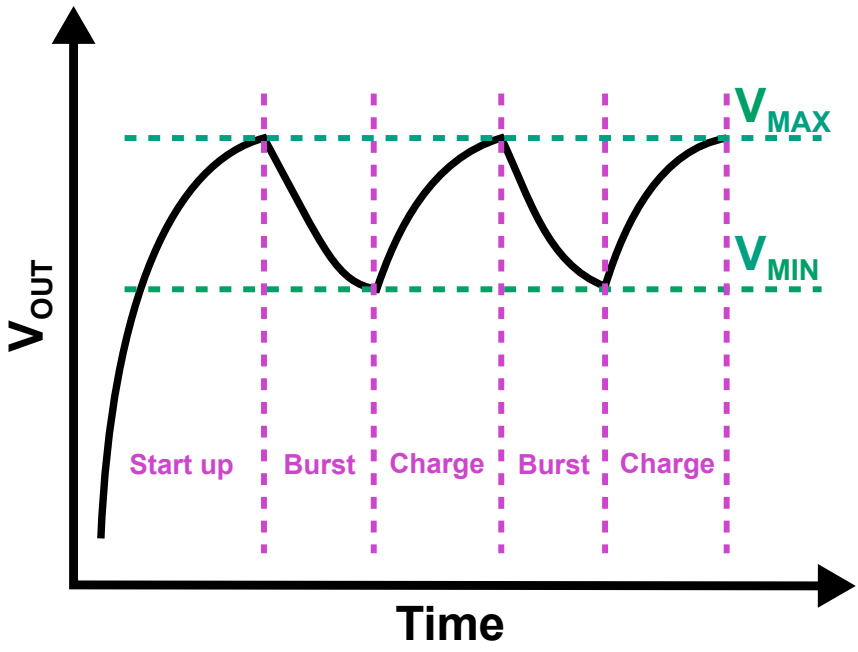


Figure 1.1. The typical waveform of a generalized charge-burst system.

additional auxiliary circuitries have to be designed to consume as little energy as possible to avoid compromising the overall system efficiency.

1.2 UHF Energy Harvesting Systems

Conventionally, the UHF harvester outputs directly to a linear regulator which then powers the system (Barnett, R. et al., 2007), as depicted in Figure 1.2 (a). An interesting trend of the recently developed energy harvesting system is that harvested energy is first accumulated over a long charge phase and then consumed in a significantly shorter burst phase, as depicted in Figure 1.1. These techniques are developed to mitigate issues with supplying power to circuits which consume significantly more than the micro-watt-level harvested power, such as a RF transceiver (Papotto et al., 2014; Stoopman et al., 2017; Papotto et al., 2018).

In addition to the charge burst technique which leverage applications where the power consumed is orders of magnitude higher than power harvested, often there is a need to manage excess energy. According to Friis energy transmission equation, in the far field, the energy transferred is inversely proportional to the square of the distance between the transmitter and receiver. As the distance between harvester and transmitter varies, the energy harvested also varies substantially. There will be instances when the harvested energy exceeds the needed energy as well as instances

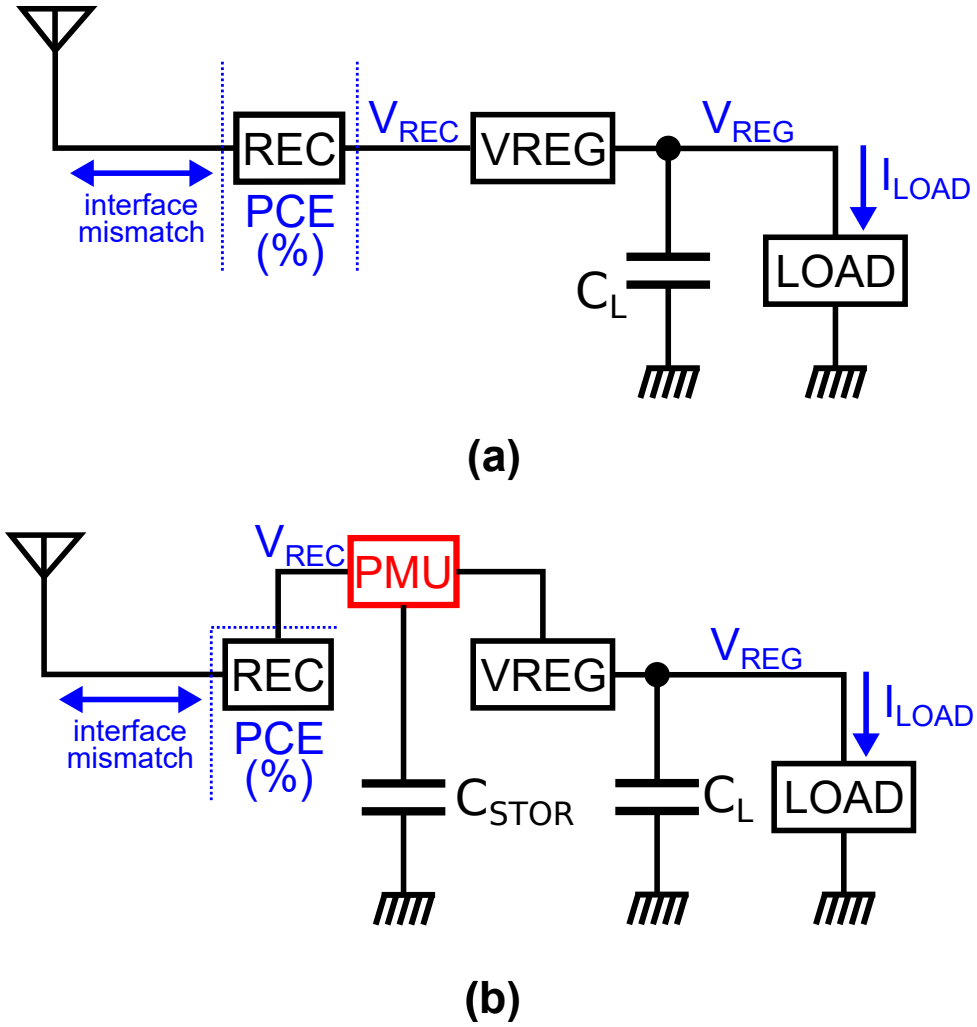


Figure 1.2. Block Diagram for PMU. (a) A conventional UHF energy harvesting system (b) An intelligent UHF energy harvesting system with the addition of a PMU.

when the harvested energy is insufficient. With the conventional approach, shown in Figure 1.2 (a), continuous operation cannot be guaranteed. If we can somehow store the excess energy when the harvested power is significantly higher than the power consumed, and then later use this energy to power the system when the harvested power is insufficient, we can potentially increase minimum input power requirement for the continuous operation of the system. This then translates to an increase in operational range of the continuous operations. This concept can be realized with the addition of a power management unit (PMU), as depicted in Figure 1.2 (b).

When continuous operation is not a requirement, to ultimately improve input power sensitivity of an energy harvester, charge-burst operations can be employed (Michelon et al., 2016). The RF-front energy harvester firstly converts a 915 MHz input power into a DC voltage across an intermediate storage capacitor and a second-stage boost

converter is used to up-convert this intermediate voltage to develop the final, much larger, boosted output voltage. There are numerous challenges in the development of this system. First of all, the front-end RF harvester needs to be very sensitive. The second stage DC booster needs to be able to operate with very low supply voltage. Thirdly, the control unit needs to reliably detect both the turn-on and turn-off threshold of the charge-burst system under the very low supply voltage developed by the front-end rectifier. Charge-burst harvester often leads to lower efficiency of the over-all system at higher input power, due to the fact that the power conversion goes through two conversion phases.

1.3 Summary of Original Contributions

The contributions made by this thesis are as follows:

1. Proposed a practical rectifier for the UHF RFID tag chip and an intuitive sizing UHF rectifier sizing schemes. The proposed design addresses key issues relating to UHF RFID tag chip, including input power sensitivity and reverse leakage. This contribution is covered in Chapter 3.

2. Proposed a simple yet efficient approaches to maintain high PCE of threshold compensated rectifier over a wide range of input power, increasing the system efficiency over most of the operating range (Sun et al., 2016). This contribution is covered in Chapter 4.

3. Proposed a simple yet efficient approach to improve settling behaviour of threshold compensated rectifier (Sun et al., 2017). This contribution is covered in Chapter 5.

4. Proposed an efficient analog solution for managing excessive power during the operation of the harvester (Sun et al., 2017,0). This contribution is covered in Chapter 6.

5. Proposed an ultra-sensitive energy harvester that is able to achieve an input power sensitivity of -40 dBm with the help of a secondary charge pump stage. This contribution is covered in Chapter 7.

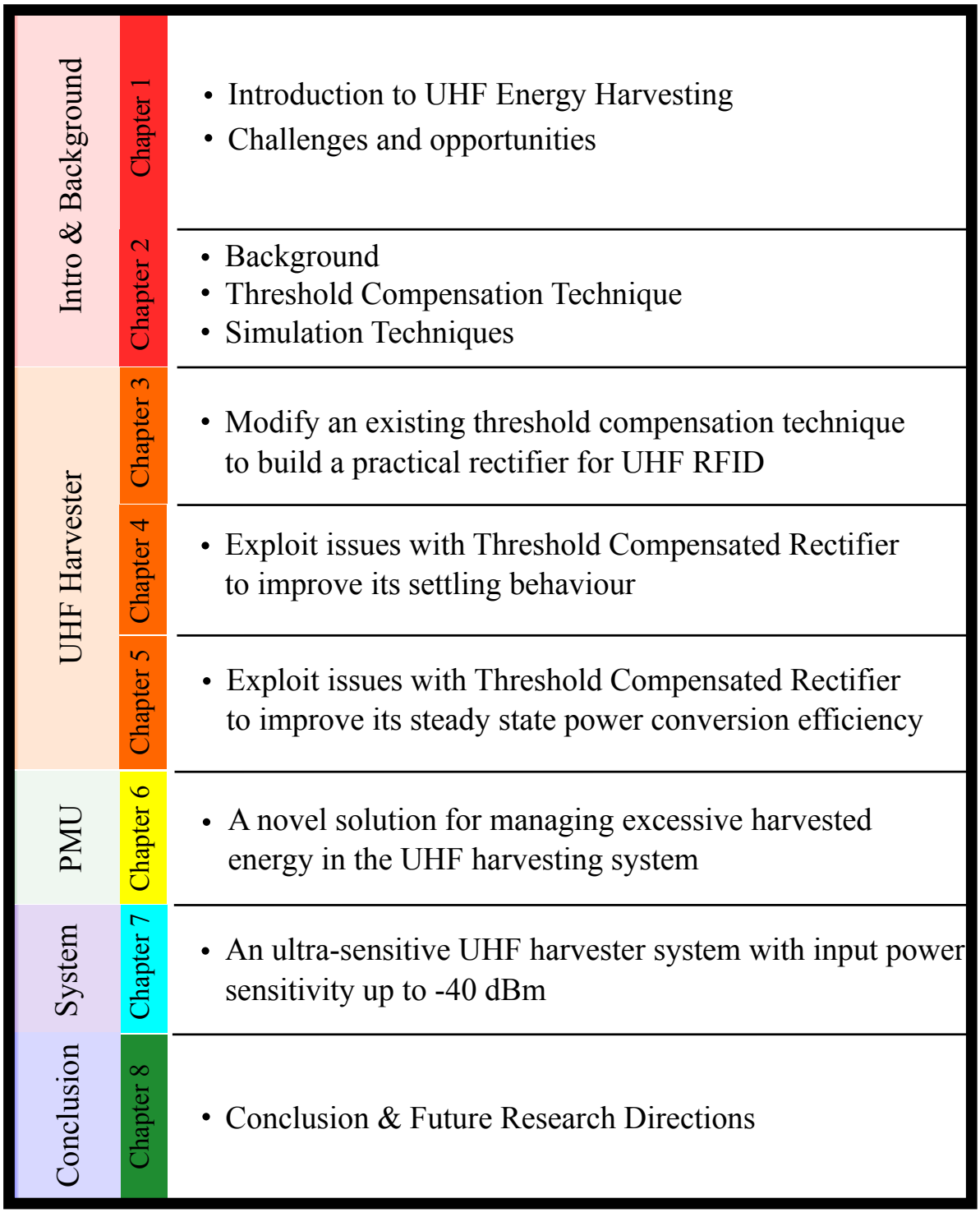


Figure 1.3. Outline of the thesis.

1.4 Thesis Structure

The aforementioned contributions of this thesis are divided into six chapters (highlighted in Fig. 1.3) and are briefly described below.

1. Chapter 2 covers the background of the low power UHF energy harvesting and threshold compensation technique is identified as a key technology in this area.
2. In Chapter 3, a recent threshold compensated circuit topology was modified to build a practical rectifier for the UHF RFID tag chip. An intuitive rectifier sizing strategy is proposed.
3. In Chapter 4, we exploit one of the fundamental properties of the threshold compensation technique to improve their settling behaviour.
4. In Chapter 5, we exploit this property again to improve the steady state power conversion efficiency of the threshold compensated rectifiers under a wide range of input power.
5. Chapter 6, we identify that there's often substantial excessive harvested power and proposed an elegant analog solution to manage this and subsequently improve the responsiveness of the harvester system.
6. In Chapter 7, we develop an ultra-sensitive UHF energy harvester with -40 dBm input power sensitivity. This is realized through boosting a primary voltage, developed by the primary RF harvester, from around 100 mV up to 1.5 V.
7. Chapter 8 concludes the thesis.

Chapter 2

Background

This chapter provides a literature view on low power UHF energy harvesting circuits. The chapter begins with a review on the mechanics of the UHF wireless power transfer and identifies the limiting factors in terms of operating range and efficiency. In addition, the threshold compensation technique, as a key technology in this area, is thoroughly reviewed and examined. Finally, simulation techniques, especially for input impedance are discussed in detail.

2.1 UHF Energy Harvesting System

2.1.1 Radiating Energy Source

As discussed in the previous chapter, one of the primary applications of the UHF energy harvester is the wireless sensor node. A typical setup of the UHF wireless sensor node is shown in Figure 2.1.

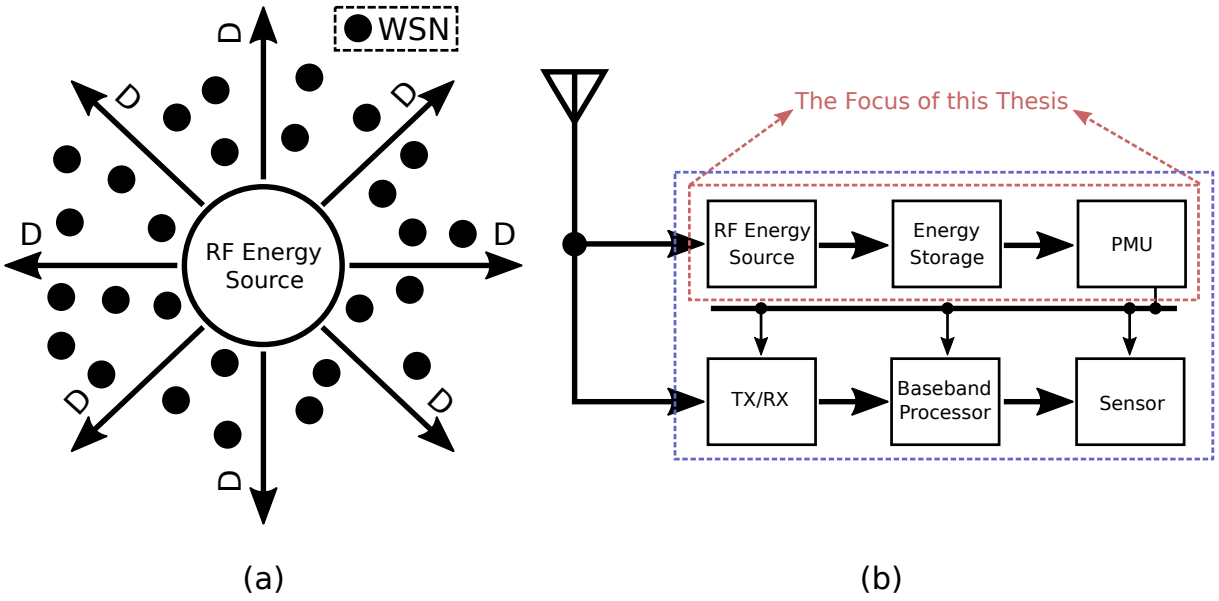


Figure 2.1. UHF energy harvesting system. (a) The base station which transfer energy to wireless sensor nodes (WSN), D denotes distance from the RF energy source (b) system-level block diagram of a wireless sensor node

As depicted in Figure 2.1 (a), the base station is radiating UHF energy in all directions (i.e. isotropically). From the study of microwave engineering, we know that the energy that is available to the wireless sensor node is significantly less for the harvester further away from the RF energy source. The available power at the harvester is often quantified by the Friis' equation,

$$P_{AV} = P_{TX} G_{TX} G_A \left(\frac{\lambda}{4\pi d} \right)^2 \tag{2.1}$$

where 2.1, P_{AV} is the available input power at the harvester. P_{TX} is the output power of the base station, G_{TX} is the directional gain of the transmitting antenna in the base station while G_A is the directional gain of the receive antenna of the harvester. $P_{TX}G_{TX}$ is often referred to as the P_{EIRP}, the Equivalent Isotropic Radiated Power. In addition,

λ and d are the transmitting wavelength and distance between the base station and harvester, respectively. It can be observed from Equation 2.1 that, the available input power decrease rapidly as the distance increases.

2.1.2 RF Interface and Rectifier Model

Given the wireless power transfer model, there is a need to develop an understanding of RF interface and rectifier model to gain insight into the receiving end of the energy harvesting system. The rectifier RF interface model is depicted in Figure 2.2. The antenna model consists of the RF voltage source V_{RF}, the real and imaginary part of the antenna impedance R_A and $-jX_A$. The antenna interface to the input terminal of the rectifier consists of the real and imaginary part, R_{REC} and $+jX_{REC}$, respectively.

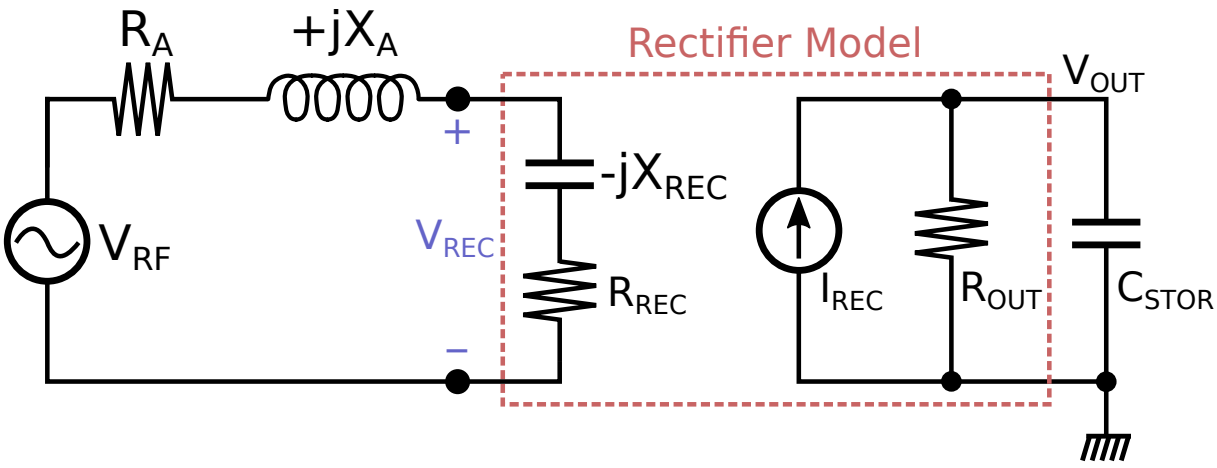


Figure 2.2. RF front-end interface and the Rectifier.

From a physical standpoint, the antenna converts the variation of the electric and magnetic fields into a RF voltage, V_{RF}, and relationship between the developed voltage and the available power is $V_{RF} = \sqrt{8R_A P_{AV}}$. For a standard off-the-shelf antenna, the real part of impedance is 50 Ω while the imaginary part of the impedance is 0. On the other hand, for most UHF rectifiers operating at low input power, the imaginary part of the rectifier impedance is orders of magnitude larger than the real part, resulting in an extremely mismatched RF interface. Thus, to achieve a better efficiency, an impedance transformation network is typically added in between the antenna and the rectifier to achieve resonance in the antenna and rectifier network (Oh et al., 2012). This exploits the high $\frac{X_{REC}}{R_{REC}}$ ratio and is used to boost the voltage amplitude across rectifier input

as shown in Equation 2.2, ultimately improving the sensitivity of the harvester and conversion efficiency at low input power. When $X_{REC} = X_A$, we have,

$$V_{REC} \simeq V_{RF} \frac{X_{REC}}{R_A + R_{REC}} \tag{2.2}$$

Note that $\frac{X_{REC}}{R_A+R_{REC}}$ is the voltage boost factor. It is possible, however, to build a custom antenna which conjugately match with rectifier's input impedance (Stoopman et al., 2014), ensuring high power transfer efficiency as well as passive voltage boosting through the resonating network.

Also shown in Figure 2.2, is the output terminal portion of rectifier model. This part mainly consists of a voltage dependent current source I_{REC} and the output Resistance R_{OUT}. I_{REC} is used to model the current pumping behaviour of the rectifier while R_{OUT} models the reverse leakage current in the rectifier chain. Thus, in reality, both I_{REC} and R_{OUT} are dependent upon the output voltage level, V_{OUT}. As this output voltage develops, the pumping current gradually decreases. When this pumping current drops to the same level as the leakage current, the output voltage V_{OUT} saturates.

2.2 Requirement of the low power UHF energy harvesting circuitry

As explained in the previous section, when the distance between the harvester and the radiating UHF source increases, the RF power that is able to reach the harvester decreases dramatically. To appreciate the implication of this, we first need to develop a circuit-level understanding of the UHF energy harvester.

In a UHF harvester, the mechanism for converting the RF power into DC power is a voltage-mode rectifier, as shown in Figure 2.3 (a). The basic voltage-mode rectifier consists of two diodes (i.e. D_1 and D_2), a coupling capacitor C_C and an output capacitor C_S, and its operational principle is described as follows. Due to the coupling capacitor C_C, V_{MID} holds the same AC phase and amplitude as V_{RF}. When the input voltage V_{RF} is in the negative phase, D_1 is forward biased and conducts, while D_2 is reverse-biased and shuts off. The charge is transferred from the ground to the middle node, V_{MID}. In the positive phase of V_{RF}, on the other hand, D_2 is forward-biased and conducts while D_1 is reverse-biased and shuts off, as such, the charge is transferred from the V_{MID} to

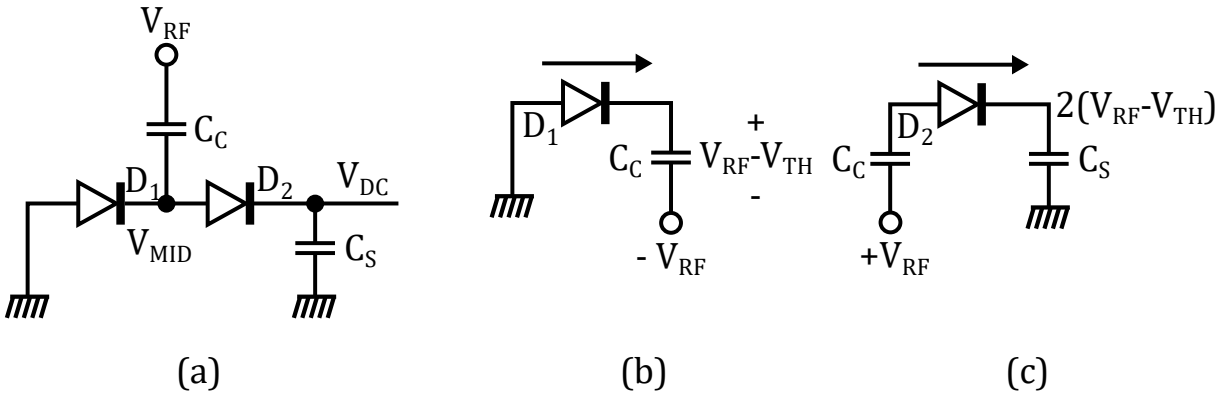


Figure 2.3. Basic diode-based rectifier. (a) A simple diagram that illustrates the operation of the voltage mode rectifier (b) The negative phase of the input V_{RF} (c) The positive phase of the input V_{RF}.

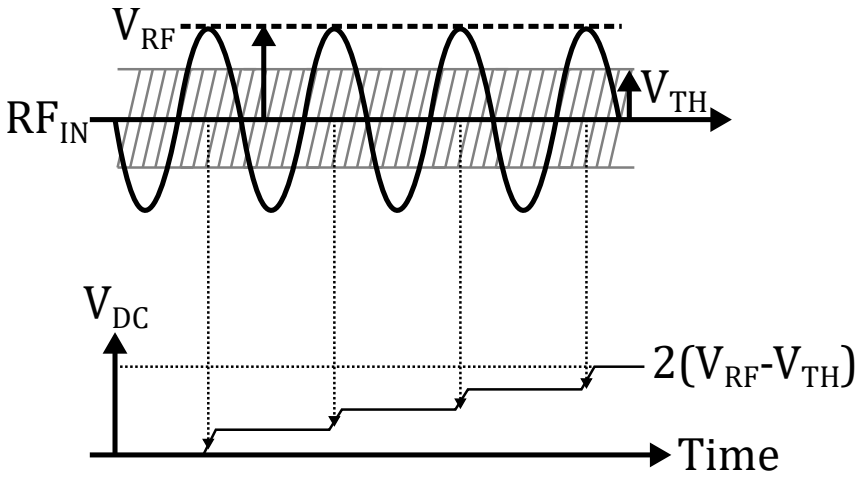


Figure 2.4. Waveform generated for the voltage mode rectifier.

the output V_{DC} and stored in capacitor C_S. Over the input RF cycles, the charges will be transferred from the ground to V_{DC} progressively and steady-state DC component of V_{MID} is half of V_{DC} if D_1 and D_2 are identical. This is the classic Dickson charge pump circuit topology and has been used for conventional voltage-mode RF rectification.

In order to identify the final settled value of V_{DC}, it is often assumed that the diode device is not able to conduct below conducting threshold V_{TH}. When V_{RF} is in negative phase, the coupling capacitor C_C is charged to $V_{RF} - V_{TH}$, as shown in Figure 2.3 (b). In the positive phase of V_{RF}, on the other hand, the node V_{MID} is charged to $2V_{RF} - V_{TH}$ and the output is thus charged to $2V_{RF} - 2V_{TH}$, as depicted in Figure 2.3 (c). Due to the finite on-resistance of the diode, the rectifier circuit will settle to the above-mentioned voltage over cycles, as depicted in Figure 2.4. The assumption we made regarding

zero-conduction below threshold is generally valid. Because, in rectifier designs, the diode devices are typically dimensioned to drive a given load in its on mode. Hence, the sub-threshold conduction for such a device is typically negligible compared to the load current.

As the harvester moves away from the energy source, both the P_{IN} input power and input voltage amplitude V_{RF} reduces subsequently. When V_{RF} falls below V_{TH} of the transistor, no output DC voltage can be established. To mitigate this problem, researchers have concentrated their effort in this area, and they have developed a class of technique called threshold compensation for UHF rectifiers, which will be discussed in the next section.

2.2.1 Threshold Compensated Rectifiers

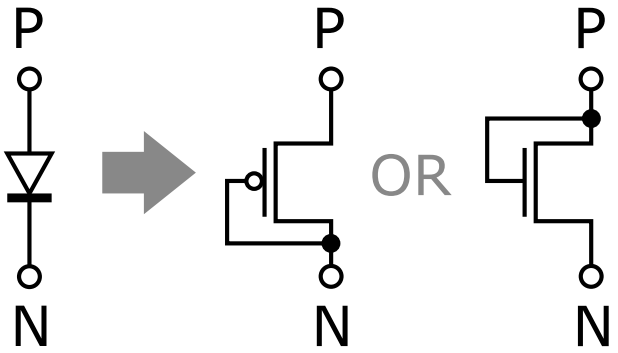


Figure 2.5. Diodes are typically implemented as diode-connected NMOS and PMOS transistor.

In a CMOS process, the diodes shown in Figure 2.3 are implemented as diode-connected transistor (NMOS or PMOS), as shown in Figure 2.5, hence the threshold voltage or the turn-on voltage of the diode is roughly the threshold voltage of the transistor. The standard threshold voltage of the low voltage transistors in typical modern technology processes is around 400 mV. For a standard 50 Ω RF interface, 400 mV RMS voltage amplitude translates to 3.2 mW or 5 dBm. However, modern UHF RFID tag or wireless sensor nodes typically requires an input power sensitivity of -10 dBm or lower (Karthaus et al., 2003; Vita et al., 2005), thus there is a need to reduce the threshold voltage.

There are many process and technology-based approaches. Such as the use of low threshold voltage transistors (Oh et al., 2012), native threshold voltage transistors (Oh et al., 2012; Karthaus et al., 2003) which provide a near zero threshold voltage. The

issue with these approaches is that they typically require special process or additional fabrication steps, thus preventing the integration into standard low-cost bulk CMOS solution.

One of the earlier circuit-based threshold compensation technique involves inserting an offset voltage that is equivalent to the threshold voltage of the transistor between the gate and source (in conduction phase) terminal of the transistor (Umeda et al., 2006), as illustrated in Figure 2.6. Hence, the threshold voltage of the devices is compensated or offset by this added voltage. From the input RF point of view, the rectifier has zero turn-on threshold voltage. The offset voltage is then generated by pushing a current into diode-connected transistor. This compensation voltage is then distributed across the gate and source terminal of transistors through a switching network (Umeda et al., 2006).

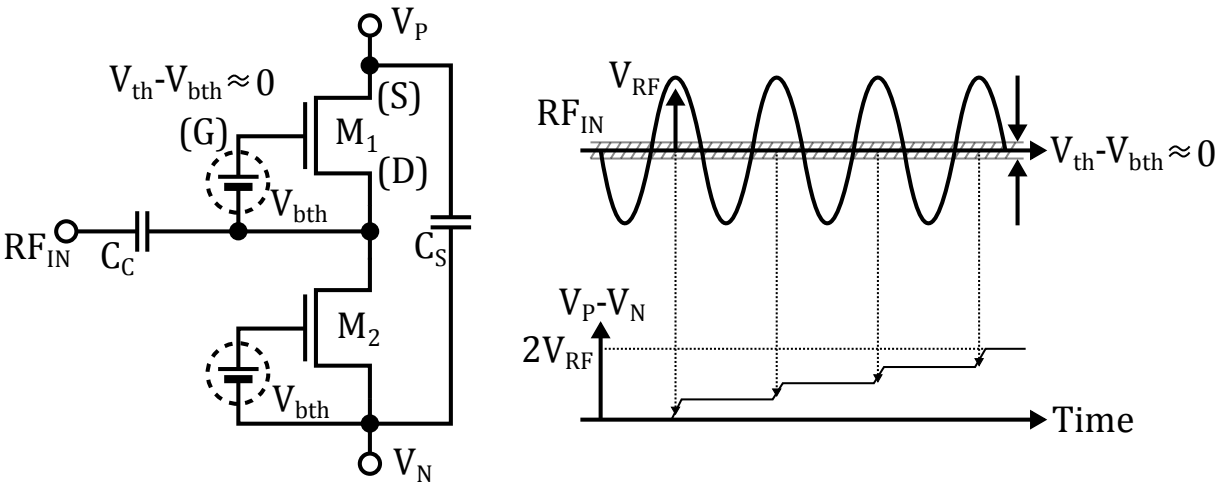


Figure 2.6. One of the first threshold compensated rectifier proposed for UHF energy harvesting application.

External generation of the compensation voltage will inevitably lead to higher power consumption and larger silicon footprint. As a result, economizing the generation of the compensation voltage is vital. As such, the internal generation of threshold compensation voltage is then proposed (Nakamoto et al., 2007), as depicted in Figure 2.7. In this circuit, transistor MN_1 and MP_1 are the main rectifying devices. Instead of tying their gates to the drain during conduction phase, the diode-connected NMOS transistor MN_2 and PMOS transistor MP_2 are being biased at their respective threshold voltage. Thus, as far as RF_{IN} is concerned, threshold voltage of rectifying devices is compensated. The current consumption of the biasing branches needs to be

minimized to ensure high efficiency of the harvester, leading to huge bias resistor and subsequently large silicon footprint.

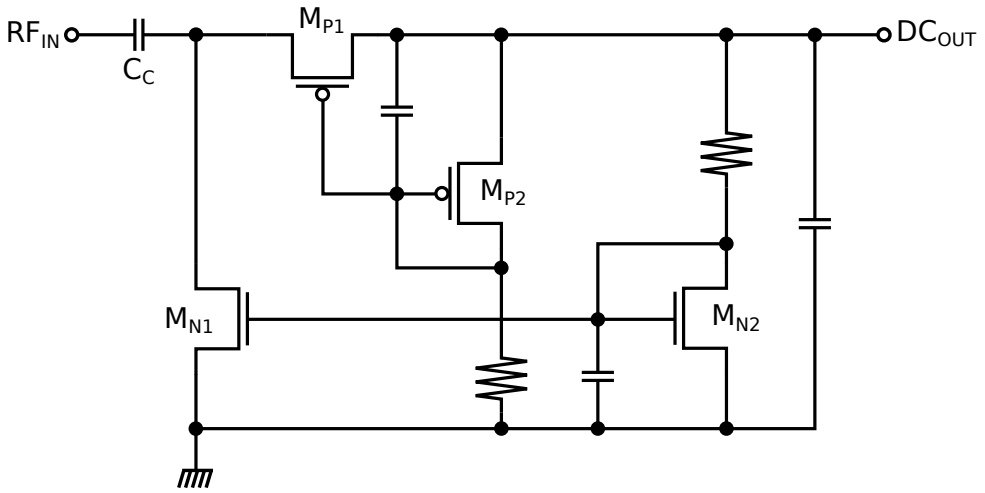


Figure 2.7. The internal compensation voltage generation technique.

To mitigate these issues, using voltages developed along the main rectification chain as the threshold compensating voltage has been explored (Papotto et al., 2011). The basic Dickson charge pump (Dickson, 1976) type voltage-mode rectifier is shown in Figure 2.8. In this basic topology, the gate terminal of the conduction device is tied to its drain terminal during the conduction phase. The issue with this configuration is that the conduction capability of the device will be hindered by the threshold voltage of the device. To mitigate this problem, the gate terminal of the conducting device is instead connected to the drain of the next stage transistor, as shown in Figure 2.9. As a result, the DC voltage of the gate terminal of the conducting device is much higher in comparison with the previous configuration. Equivalently, the threshold voltage of the conducting device can be considered as to be compensated by the DC voltage of a single charge pump stage. This is termed as ”level-1” compensation.

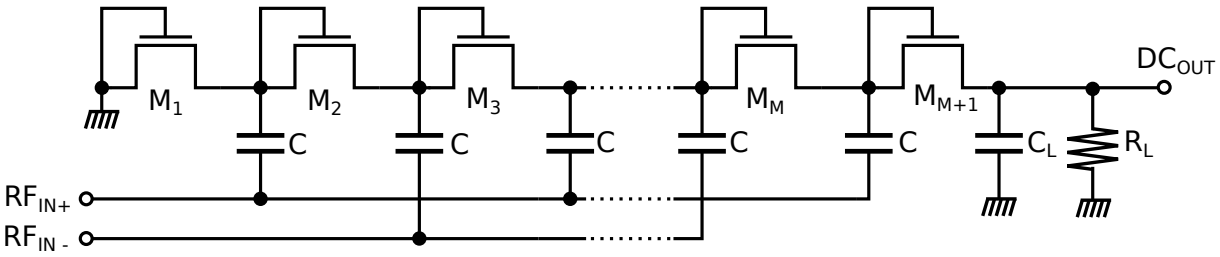


Figure 2.8. The basic Dickson charge pump circuit topology used for voltage mode rectification.

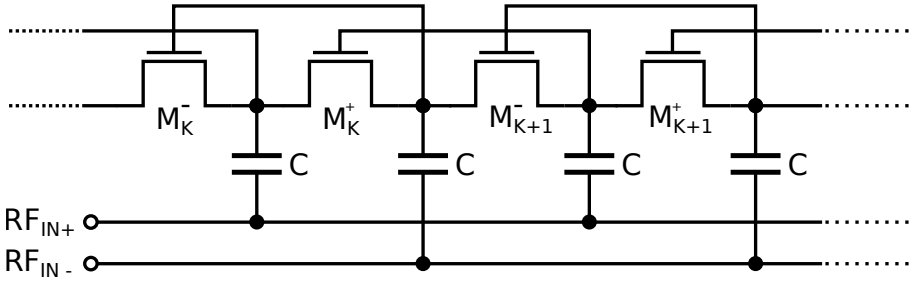


Figure 2.9. The improved Dickson charge pump circuit topology with level-1 threshold compensation.

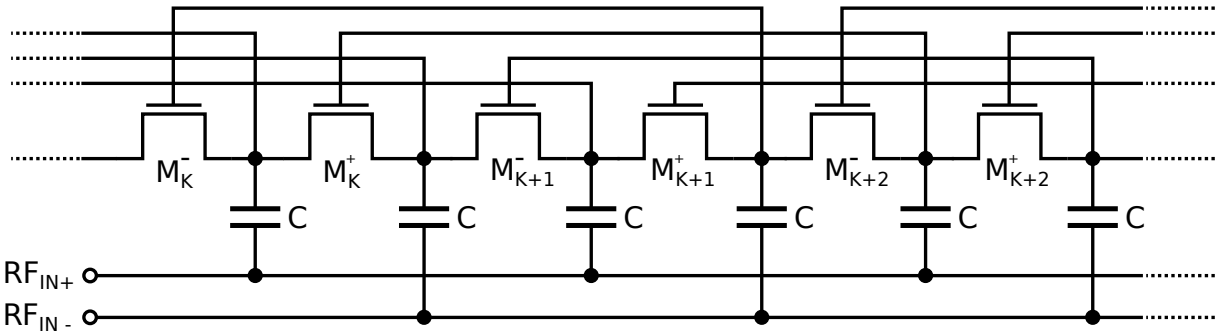


Figure 2.10. The basic Dickson charge pump circuit topology used with level-2 threshold compensation.

This idea of threshold compensation can be expanded to further reduce the equivalent threshold voltage of the conducting device, as shown in Figure 2.10, where the gate terminal of the conducting device can be connected to the third next stage device. Note that subscript here represents the charge pump stage number while superscript denotes the phase during which the rectifying device is one. Hence M_K^+ stands for a rectifying device in Kth charge pump stage which only conducts during the positive phase of the RF input. In this circuit, the gate voltage of each rectifying transistor is compensated by the DC voltage of two charge pump stages. This is particularly useful when the input amplitude is very small and the develop DC voltage of a single charge pump stage is insufficient to compensate the threshold voltage of the rectifying transistor.

This concept can be further extended to create a higher order threshold compensation (e.g. level-3 compensation) where the gate voltage comes from a higher DC node (Papotto et al., 2011), as depicted in Figure 2.10. However, this causes excessive reverse leakage with moderate input amplitude, resulting in poor PCE for the most part of the input power range.

In the previously discussed circuits techniques, the threshold voltage of the rectifying device has always been in one direction and their threshold voltage statically reduced. While this is desirable in the conduction phase, the device will leak current in the shut-off phase without its intrinsic threshold voltage. As such, it is often considered more efficient for the threshold voltage to be compensated in both directions. Specifically, when the rectifying device is conducting, the threshold voltage is backward compensated, reduced. On the other hand, when the rectifying device shuts off, the threshold voltage of the device is forward compensated, increased. Overall, more charge can be pushed to the output capacitor over one period compared to the threshold compensation scheme where the threshold voltage compensated in a single direction. Such a threshold compensation scheme can be easily implemented in differential rectifier circuit and one of most commonly used differential threshold compensation topologies is the cross-coupled inverters (Kotani et al., 2009), which is shown in Figure 2.11.

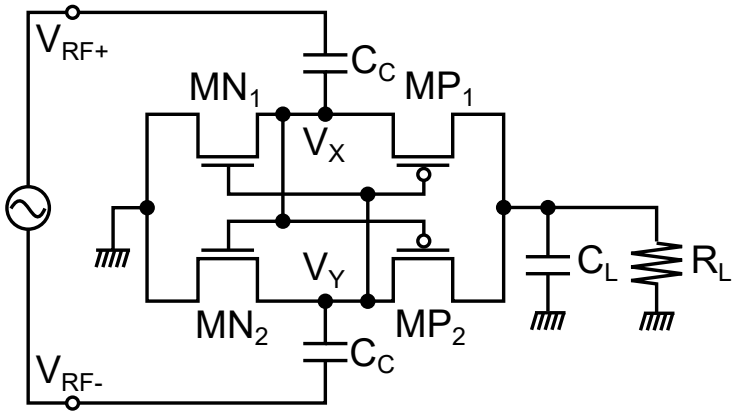


Figure 2.11. The differential rectifier circuit topology which compensates threshold voltage in 2 directions (Kotani et al., 2009).

As can be observed in Figure 2.11, in the positive phase of the input RF, MP_1 is in conduction phase and MN_1 is in shut-off phase, the negative V_Y reduces the effective threshold voltage of MP_1 and increases the effective threshold of MN_1, maximizing the conduction current through MP_1 and minimizing the leakage current through MN_1. In the negative phase of the input RF, on the other hand, MN_1 is in conduction phase while MP_1 is in shut-off phase, the positive V_Y increases the effective threshold voltage of MP_1 and decreases the effective threshold of MN_1, minimizing the reverse leakage current through MP_1 and improving forward conduction MN_1. Since the threshold voltage are compensated differently in the two phases of the input, this scheme is

also referred to as dynamic threshold compensation, opposed to the static threshold compensation in circuit techniques discussed previously.

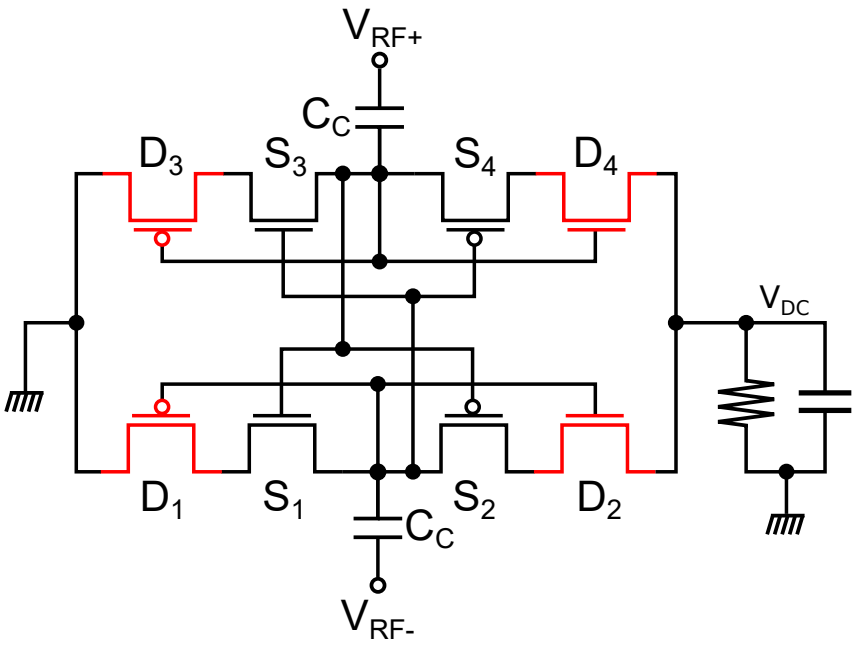


Figure 2.12. A modified version of the cross-bridge rectifier proposed in (Kotani et al., 2009).

Shown in Figure 2.12 is a modified version of cross-bridge rectifier proposed in (Theilmann et al., 2012). In this differential circuit, the rectifying device is a mix of the standard diode-connected transistor (denoted by D_1 to D_4) and cross-connected transistors (S_1 to S_4). In this work, native transistors were employed to further reduce the input turn on threshold of the rectifier. However, drawback of this device choice is that the leakage during the shut-off phase of the rectifying device is huge. Theilmann et al. (Theilmann et al., 2012) proposed to add a complementary transistor (highlighted in red) to suppress the reverse leakage. During the positive phase of the RF input, S_3 is in shut-off, the gate source voltage of the transistor D_3 is reverse-biased, providing excellent isolation from ground. In the negative phase of the RF input, S_3 is in conduction phase, thus the gate of D_3 is shorted to its drain, forming a diode-connected transistor. Since the threshold of the native transistor D_3 is close to 0, the complimentary transistor D_3 does not limit the conduction capability of S_3. The same principle applies to the other three pairs of transistors.

The differential topology requires the two input RF pins and fully balanced differential antenna, which may not be always possible in a real application scenario. Recent effort (Hameed et al., 2015) have demonstrated a single-ended rectifier that also

achieves bi-directional threshold compensation, the design is depicted in Figure 2.13. In the negative phase of the V_{IN}, the auxiliary transistor M_{NB} (PMOS) turns off, which shorts the gate of M_N (PMOS) to the input node of the previous stage to reduce threshold voltage. In the positive phase of the V_{IN}, the auxiliary M_{NB} turns on, connecting the gate of M_N to the input node of its own stage to cancel out the threshold voltage reduction and reduce reverse current leakage.

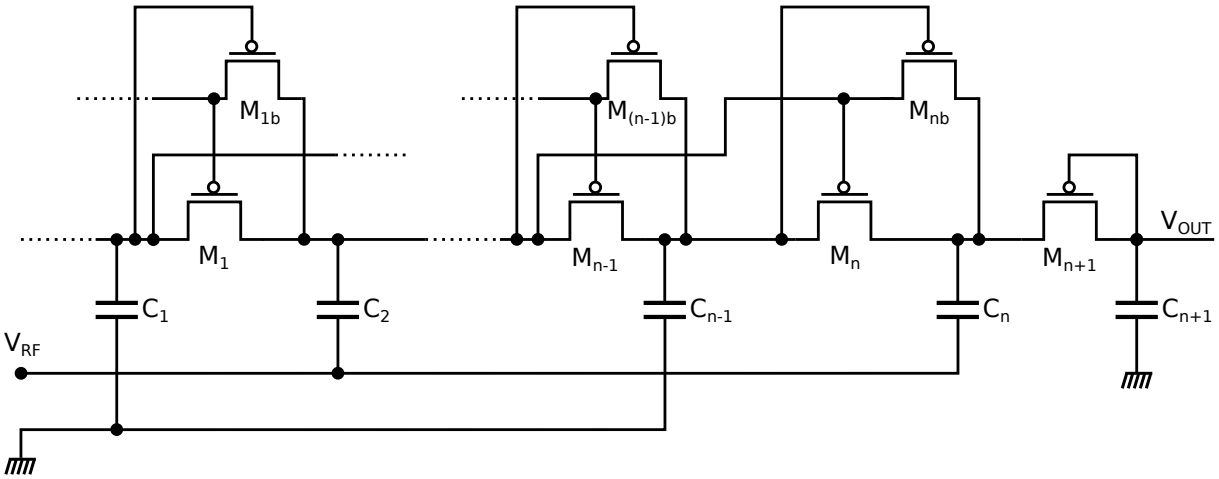


Figure 2.13. A single-ended rectifier with bi-directional threshold compensation (Hameed et al., 2015).

2.3 Simulation Techniques

Both Transient and PSS simulation techniques are indispensable tools for the design of UHF energy harvester. As such, in this section, they are discussed in detail in the context of UHF energy harvesting system.

2.3.1 Transient Approaches

The advantage of the transient approaches is that the full transient behaviour can be simulated. In this approach, the establishment of the final DC voltage is the complicated progressive interaction between the RF interface and the rectifier circuit behaviour. However, if only steady state conditions are needed, PSS is preferred over full transient analysis due to the significantly shorter simulation time, as illustrated in Figure 2.14.

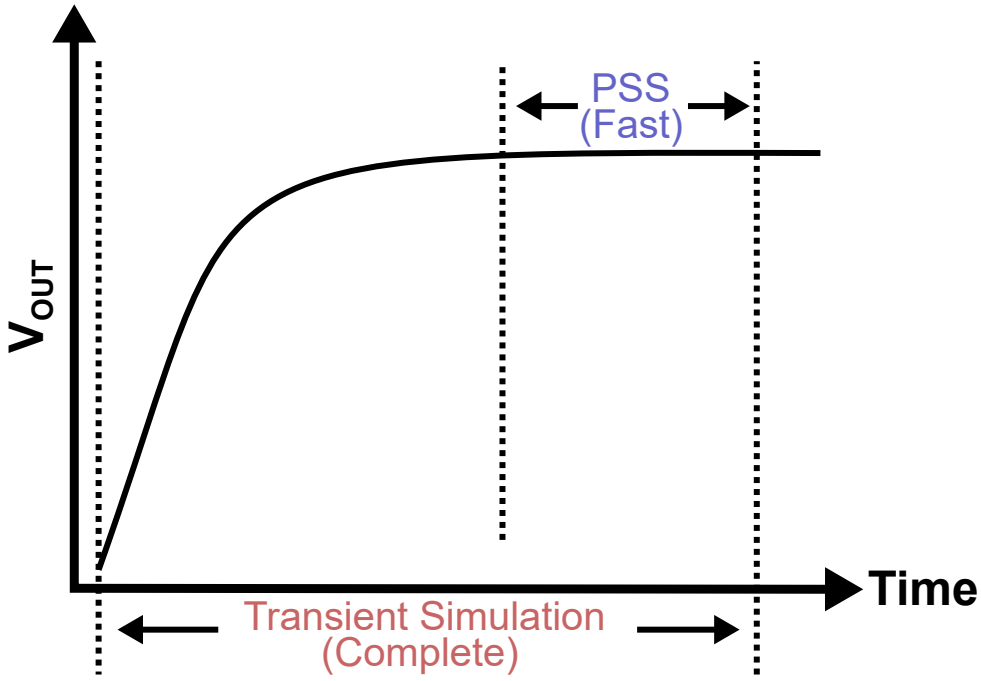


Figure 2.14. The transient simulation vs periodic steady-state simulation for UHF rectifier.

A typical set-up for the transient simulation for the UHF energy harvester is shown in Figure 2.15. The reactive part of the source is emulated through the inductor and the real part of the source is emulated through the resistor part of the port element. The advantage of using the port element is that we can specify the input power level, which allows for the modelling of the real interface behaviour in the transient simulation. For a fixed source impedance (specified by the resistor and inductor), the input impedance of the rectifier and the input amplitude across the rectifier change as the rectifier output settles. In addition to the interface behaviour, the dynamic behaviour of power conversion efficiency can also be obtained with a given resistive load. Note that it is possible to specify a port element with a complex impedance, however, this is only allowed in harmonic balance frequency-domain simulation, thus it is better to use a separate inductor to realize this positive reactants (i.e. $+j$) to make the test-bench reusable for both time-domain and frequency-domain simulation.

The way we compute the dynamic input impedance of the rectifier is to measure the RF voltage at the source and rectifier interface and the RF current flowing into the rectifier. Since the obtained transient waveform are time-domain data, we can then compute the FFT value of the voltage at the input of the rectifier and the current into

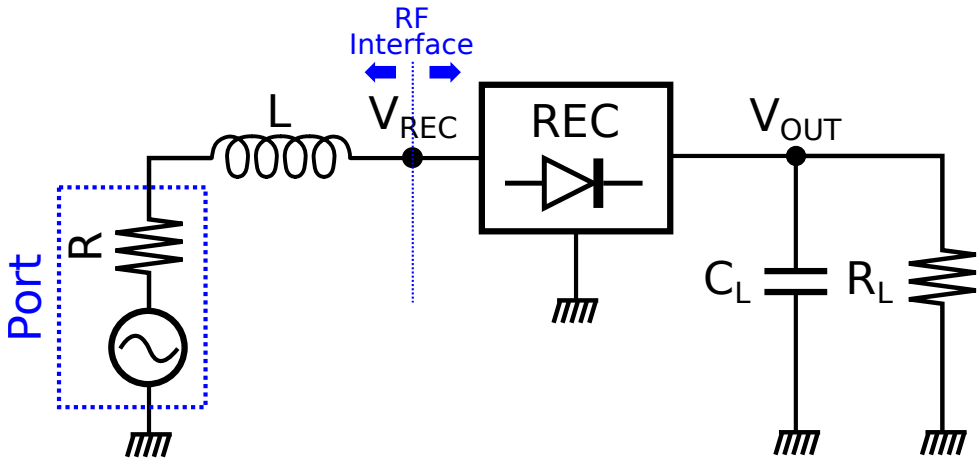


Figure 2.15. The simulation setup for the transient simulation for UHF harvesters.

the input of the rectifier, V_{REC} and I_{REC}. Finally, the input impedance into the rectifier Z_{REC} is simply (Pellerano et al., 2010),

$$Z_{REC} = \frac{V_{REC}}{I_{REC}} \tag{2.3}$$

Note that the FFT needs to be computing over the time period centred around the time instance for which Z_{REC} is computed, which is illustrated in Figure 2.16.

2.3.2 Periodic Steady State Analysis Approaches

In Cadence, the periodic steady-state analysis can be employed to compute the steady state behaviour of the circuit under periodic operation. As discussed previously, PSS is especially useful for the design of UHF rectifier, because the transient simulation takes a long to finish due to its high operating frequency. In this thesis, the harmonic balance option of the PSS is chosen to enable full frequency-domain analysis. In this simulation mode, circuit properties, such as node voltage and branch current, input impedance are readily available. One obvious drawback of this approach is that it does not provide any insight into the settling behaviour which lead to the steady state. However, since computing the input impedance in transient simulation requires manual operations (e.g. finding the right time interval, choosing the right number of samples), results obtained from PSS can serve as a sanity check. Specifically, it is a good practice to compare the input impedance computed for the settled (i.e. steady-state) portion of the transient waveform to the input impedance from PSS analysis to check if the FFT has been configured in a proper manner.

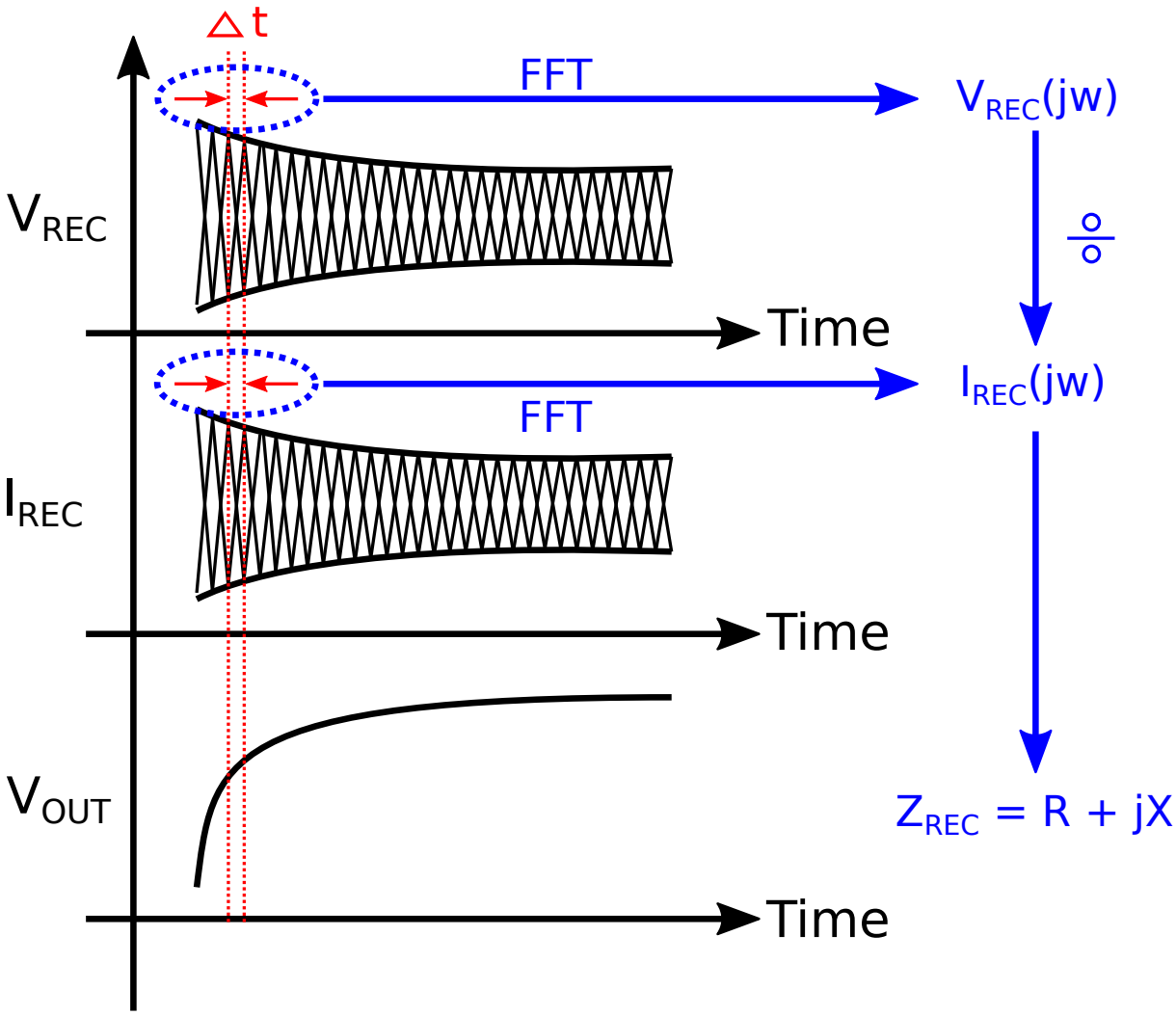


Figure 2.16. A diagram that illustrates the procedure for real time input impedance of the rectifier in transient simulation.

2.3.3 Simulating with ideal voltage sources

It has to be noted that it is sometimes also useful to simulate the rectifier circuit with an ideal voltage source. For example, there is often a need to work out the intrinsic behaviour of the rectifier circuit, such as the power conversion efficiency at a given input amplitude. Additionally, the utilisation of an ideal source can be a time saver when there is a need to conduct intermediate simulations. For example, in cases where we already know the voltage amplitude that can be developed across a given rectifier and power source interface in steady state, we can simply feed this voltage at the interface. The results of this short-cut transient simulation, however, does not capture the full transient behaviour of a physical harvester. Nonetheless, the developed output

voltage can influence interface behaviour, and effectively the voltage amplitude at the interface, in real time. Hence, this continuous change of the interface behaviour is not captured.

2.4 Conclusion

Threshold voltage compensation technique builds the foundation for low power UHF energy harvesting as it enables significant input power sensitivity improvement without relying on the typically expensive technology-based approaches (Karthaus et al., 2003). Understanding the RF interface and relevant simulation techniques are crucial to the design of UHF energy harvester. Through the rest of the thesis, this knowledge will be employed and built upon to tackle some of the key challenges in the field of low power UHF energy harvesting. In the next chapter, we start with applying the threshold compensation technique to build a practical UHF energy harvester.

Chapter 3

An Ultra-Sensitive Differential Rectifier for UHF RFIDs

THIS chapter presents an ultra-sensitive rectifier design, which is optimized to boost the input power sensitivity of the UHF RFID tag chip. In the post-layout simulation, the proposed 5-stage rectifier is able to develop 1 V across 1 MΩ resistor at −27.6 dBm input power level at 915 MHz, with a maximum power conversion efficiency (PCE) of 66 %.

3.1 Introduction

Passive Ultra High Frequency (UHF) Radio Frequency Identification (RFID) is gaining tremendous popularity in recent years. Key features of passive UHF RFID are the long read range of transponders that do not rely on batteries and the ability to read hundreds of co-located tags simultaneously (Finkenzeller et al., 2010). A crucial component to achieving such desirable performance is the PCE of the rectifier to convert incident RF power to DC and the threshold voltage required at the input of the rectifier to turn on rectification. Therefore, reducing the turn-on voltage of the rectifiers to achieve a higher sensitivity is an important design goal. In this chapter, we exploit threshold compensation, in particular dynamically varying the voltage potential between the source and bulk terminals of a MOSFET, to realize a highly sensitive rectifier for RF to DC conversion. Given the higher sensitivity of differential rectifier topologies, we design a multi-stage differential-drive rectifier suitable for UHF RFIDs.

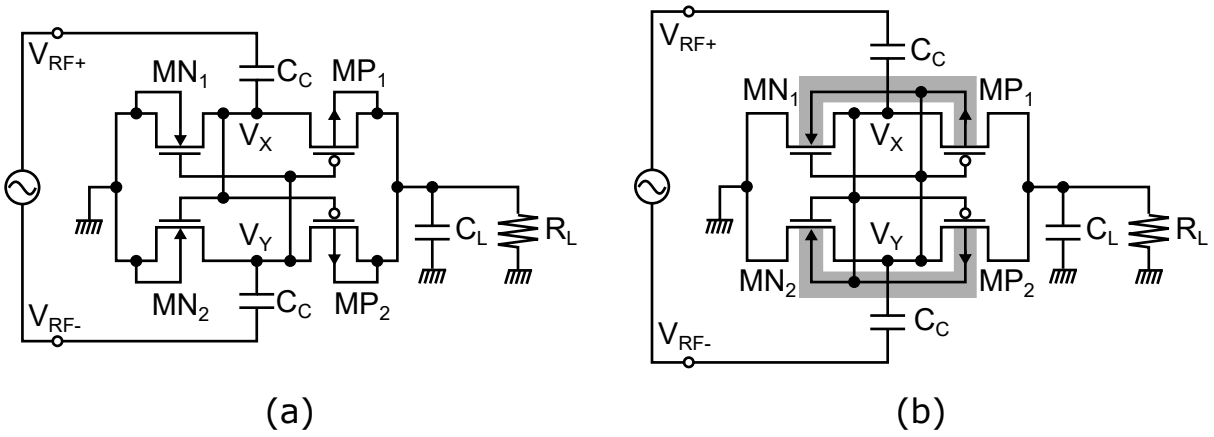


Figure 3.1. Differential-drive threshold compensation techniques. (a) conventional approach (b) improved approach

3.2 Threshold Compensation Techniques

The differential-drive threshold compensation technique (Kotani et al., 2009) introduced in Chapter 2, depicted in Figure 3.1(a), has been established as a very efficient approach to implement rectifiers with high sensitivity. In this circuit, the threshold voltage of the transistors is compensated for in a dynamic manner. Take

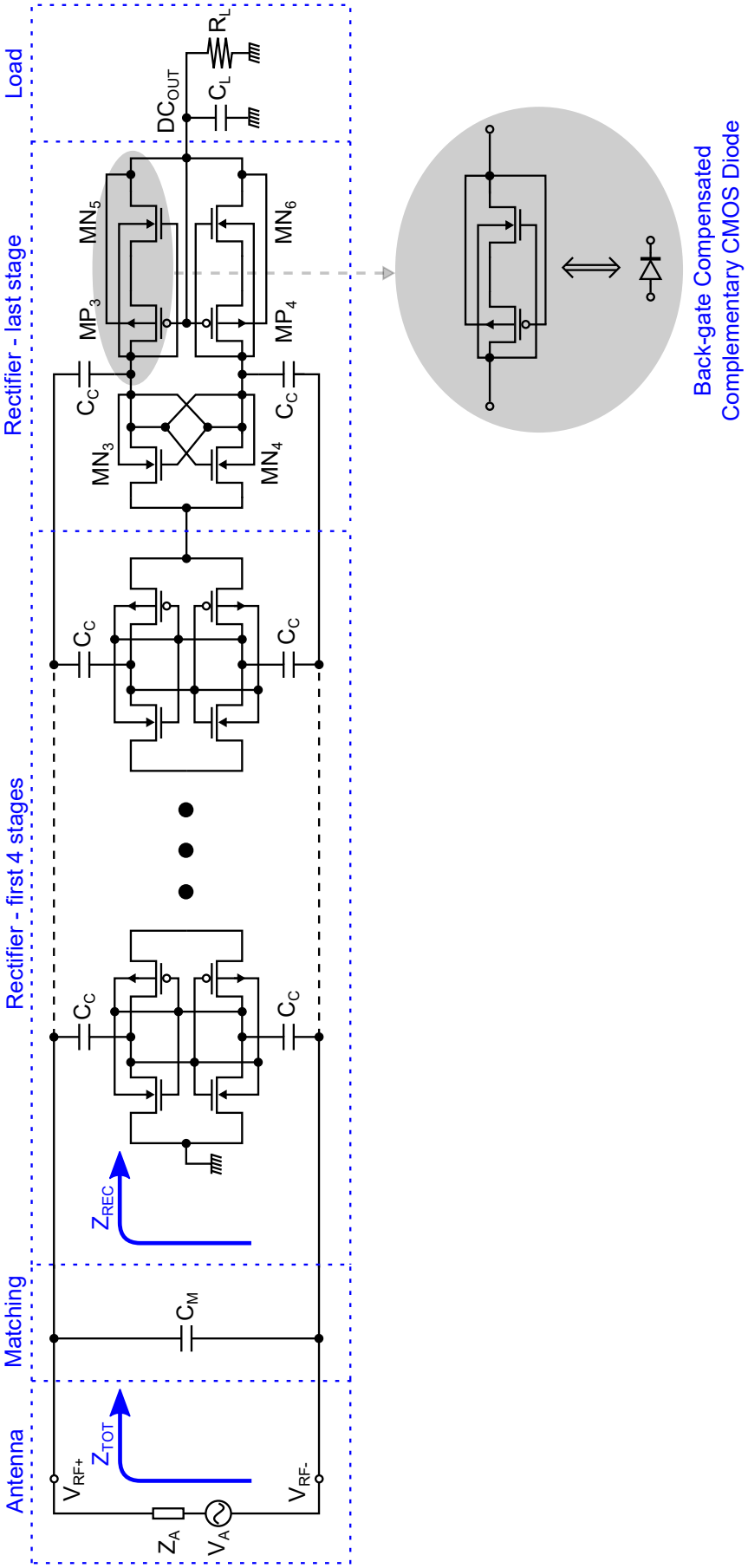


Figure 3.2. The proposed 5-stage rectifier.

MN_1 for example, during the negative cycle, where V_{RF+} and V_X are negative and V_{RF-} and V_Y are positive, the transistor is in conduction mode and the voltage needed to turn on the transistor is provided by the positive gate voltage at V_Y. Similarly, during the positive cycle, the transistor is in cut-off mode and the voltage needed to turn off the transistor is provided by the negative voltage at V_Y. Thus, this structure is very effective in the design of highly sensitive rectifier as it achieves improved forward conduction and reduced reverse leakage simultaneously.

It is well understood that the threshold voltage of a MOSFET can be adjusted by varying the voltage difference between the source and bulk terminals, V_{SB}, given by (Razavi et al., 2001),

$$V_{TH} = V_{TH0} + \gamma \left(\sqrt{|2\Phi_F - V_{SB}|} - \sqrt{|2\Phi_F|} \right) \tag{3.1}$$

where V_{TH0} denotes the threshold voltage with $V_{SB} = 0$, and γ and Φ_F are technology-dependent parameters. This opens up the possibility for further threshold compensation through the bulk terminal, which is exploited by the circuit topology shown in Figure 3.1(b) (Chouhan et al., 2015). During the negative cycle where V_{RF+} is negative and V_{RF-} is positive, V_{SB} of MN_1 is negative because the bulk terminal is connected to V_Y. This reduces the V_{TH} of MN_1 according to Equation 3.1. During the positive cycle where V_{RF+} is positive and V_{RF-} is negative, V_{SB} of MN_1 is positive, increasing the V_{TH} of MN_1. On the other hand, during the positive cycle, the polarity of V_{SB} is reversed, decreasing V_{TH} of MN_1 according to Equation 3.1. Overall, due to the bulk connection, the threshold voltage decreases during the negative cycle when the device conducts and the threshold voltage increases during the positive cycle when the device shuts off. Hence, overall, the rectifying device conducts more current in its forward conduction phase and leaks less current in the shut-off phase.

3.3 Proposed Rectifier Design

In this work, we use the improved differential-drive threshold compensation technique depicted in Figure 3.1(b) to design a practicable rectifier for UHF RFID tag chips, as shown in Figure 3.2. Both the design procedures and practical considerations are discussed in detail in this section.

3.3.1 Sizing of the single stage rectifier

Sizing and optimizing of the UHF rectifier is a complicated task. There are mainly two reasons for this. Firstly, there are a large number of elements that need to be optimized. For example, there is the input coupling capacitor, the width and length of the NMOS and PMOS transistors and the number of stages. Secondly and more importantly, due to inherent non-linearity of the rectifier circuit, the trade-off between these elements cannot be easily quantified using linear circuit theory. Brute-force simulation approaches can be extremely time-consuming and can easily lead to sub-optimal solution. As such, it is therefore necessary for circuit designers to make creative and educated simplification to gain design insights.

Firstly, minimum length (i.e. 130 nm) is chosen to ensure optimum RF performance and minimum R_{ON} during conduction. Secondly, due to difference in mobility between the NMOS and PMOS transistor, the width of the PMOS is sized to be 2.6 times larger than that of the NMOS. Thus, effectively, the only remaining sizing task is to determine the width of the NMOS transistor. The width of the transistor determines the current pumping capability of the rectifier given the input amplitude and the load. To start the analysis, the voltage efficiency (V_{OUT}/V_{IN}) against V_{IN} is plotted in Figure 3.3.

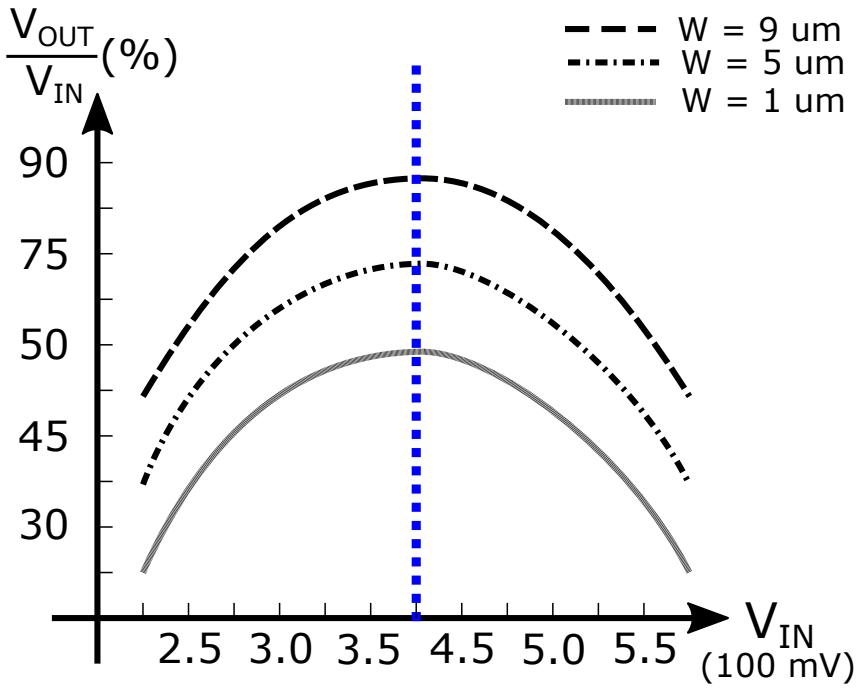


Figure 3.3. Voltage Efficiency against input voltage amplitude for a 10 kΩ load.

It can be observed in Figure 3.3 that the shape of each curve is roughly the same and the maximum achievable voltage efficiency (V_{OUT}/V_{IN}) happens at the same input voltage amplitude, irrespective of the transistor width. Thus we can then collect the peak voltage efficiency (V_{OUT}/V_{IN}) for a set of output load and transistor width and plot these data in terms of voltage efficiency and width, as depicted in Figure 3.4.

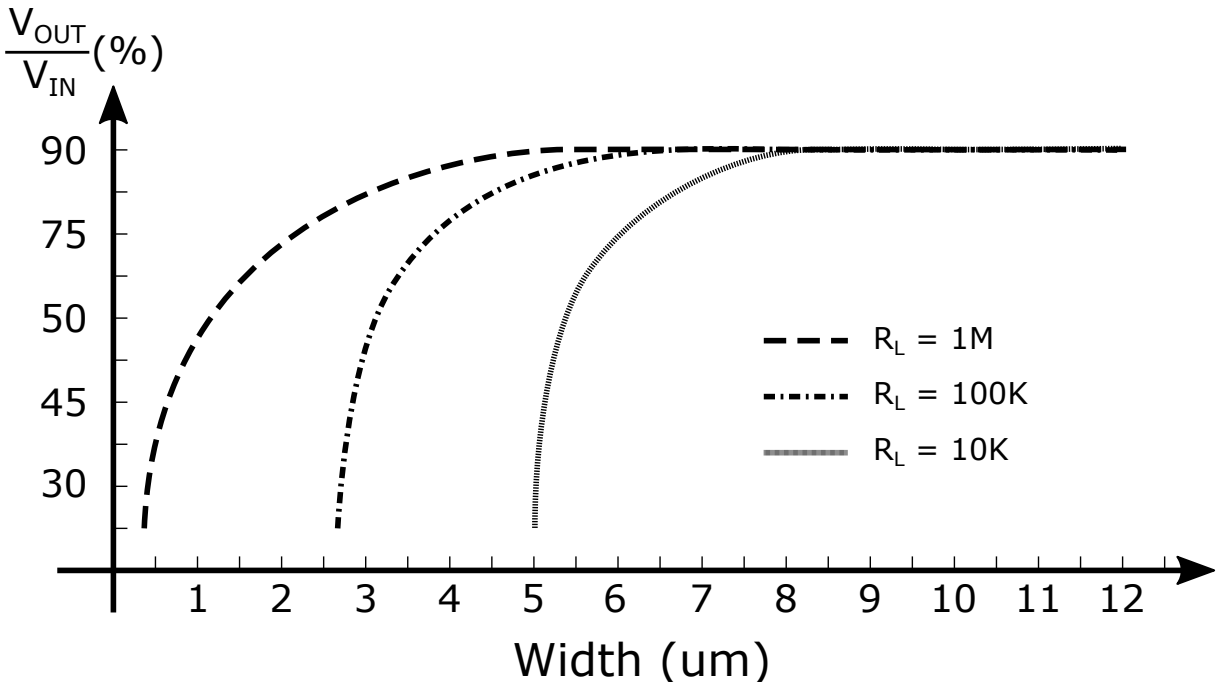


Figure 3.4. Peak Voltage Efficiency against transistor width for a number of load.

From Figure 3.4, it can be observed that the peak voltage efficiency for a particular load tends to flat out as the width of the rectifying transistor increases. When the load current is low (i.e. large load resistor), the voltage efficiency tends to flat out at a relatively small transistor width. One the other hand, the voltage efficiency tends to flat out at a relatively large transistor width when the load current is high.

Although the voltage efficiency flats out, it is not desirable to choose a larger than necessary device, because an excessively larger device results in more reverse leakage, leading to poor power conversion efficiency. On the hand however, it is generally desirable the transistor is sized to be sufficiently deep into the flat region of the voltage efficiency curve, so that the voltage efficiency performance of the rectifier is more robust with process variation. In this work, the dimensions $W_{NMOS} = 10\,\mu m$, $W_{PMOS} = 26\,\mu m$ and $L_{NMOS} = L_{PMOS} = 130\,\text{nm}$ are selected, in order to cope with a load down to 10 KΩ load. Each of the four transistors is divided into 8 fingers to

minimize parasitic capacitance and gate resistance and deep-n-well is used so that the bulk terminals of both NMOS and PMOS can be connected to their gate terminals. Lastly, 1 pF MIMCAPs are used to realize the coupling capacitors C_C to minimize substrate loss and capacitive voltage division.

3.3.2 Multi-Stage Rectifier

In this design, a separate deep-n-well is used for each rectifier stage so that the well potential could be tied locally within the stage. Because of the use of deep-n-well, we have eliminated the increased threshold voltage in latter stages in a multi-stage rectifier due to body effect. As shown in Figures 3.3 and 3.4, the optimal voltage efficiency achieved at around 0.4 V with a voltage efficiency of around 80%. In this work, the rectifier is designed to output around 1 V to 2 V, thus a total of 5 stages are configured in series to provide of the final output voltage, as depicted in Figure 3.2.

A practical rectifier should be able to retain the charge in the output capacitor in case of a sudden drop in the input power. This is commonly addressed by designing the last stage of the rectifier with a conventional diode-connected transistor or a complementary MOS diode as discussed in (Papotto et al., 2011) and (Stoopman et al., 2014), respectively. In the proposed design, we implement the last stage with a modified complementary MOS diode that exploits the dynamic back-gate biasing to achieve lower turn-on voltage and higher current conduction capability with small input voltage amplitude. Specifically, as shown in Figure 3.2, the bulk terminal of MN_3 and MN_4 are tied to the RF input on their opposite side to achieve threshold-reduction during its conduction phase and threshold-enhancement during its shut-off phase. On the other hand, since the conduction phase for MN_5 and MN_6 are opposite to that of MN_3 and MN_4, their bulk terminals are connected to the RF input on their own side rather than the opposite side to achieve the same threshold compensation as with MN_3 and MN_4. In addition, the bulk terminals of MP_3 and MP_4 are tied to DC_{OUT}, which results in a positive V_{SB} during its conduction phase and reduces the threshold voltage of these two PMOS transistors. In the event of a sudden power drop, the V_{SB} of MP_3 and MP_4 are negative whereas that of MN_5 and MN_6 are positive. Therefore, the threshold voltages of both NMOS and PMOS transistors are increased and subsequently the reverse leakage current is minimized.

3.3.3 RF Interface Considerations

Due to the differential nature, the input impedance of the differential-drive rectifier circuit is highly reactive. However, it is challenging to design an RFID-label-size antenna with a large reactance to provide a conjugate impedance match (Balanis et al., 2016). To mitigate this, we add a shunt matching capacitor C_M, as shown in Figure 3.2, to reduce reactance of the rectifier's input impedance.

Specifically, at the turn-on threshold (i.e. $V_{RF+} - V_{RF-} = 300\,mV$), using the technique introduced in the last chapter, the simulated input impedance of the 5-stage rectifier at 915 MHz with a 1 MΩ is $Z_{REC} = 65 - j1200\,\Omega$. Therefore, the matching capacitor is set to $C_M = 350\,fF$ to transform the input impedance to $Z_{TOT} = 3.8 - j362\,\Omega$. In order to provide a conjugate match to the rectifier's input impedance at minimum input power, the antenna impedance is set to $Z_A = 3.8 + j362\,\Omega$ at 915 MHz. Using similar approaches, the optimum source impedance for 100 KΩ and 10 KΩ load have been calculated to be $Z_A = 21 + j102\,\Omega$ and $Z_A = 52.5 + j76\,\Omega$, respectively.

3.4 Simulation Results

The rectifier is realized in Globalfoundaries 130 nm Generic process. The post-layout simulation is conducted in Cadence Virtuoso design environment. All possible passive parasitics, including those associated with coupling capacitors and input pads, are taken into account and they are accurately generated in the 3D field-solver-based parasitic extraction mode. In addition, to compare the performance of the proposed rectifier design with others presented in the literature, sensitivity is defined as the available power from the antenna required to achieve 1 V across a 1 MΩ load resistor, because we expect the digital section of the UHF RFID tag chip to consume 1 μW (Vita et al., 2005). PCE is defined as, $PCE = (P_{OUT}/P_{AVA}) \times 100\%$, where P_{OUT} is the output DC power and P_{AVA} is the available power at the antenna.

The simulated PCE of the proposed 5-stage rectifier is presented in Figure 3.5. It is noted that PCE and output voltage for each of three loads (i.e. 1 MΩ, 100 kΩ and 10 kΩ) are simulated with their respective optimum source mentioned. This is because as the load increases, the input impedance of the rectifier changes and therefore the rectifier-antenna interface becomes mismatched. In Table 3.1, the performance of the proposed rectifier is compared with the results reported in the

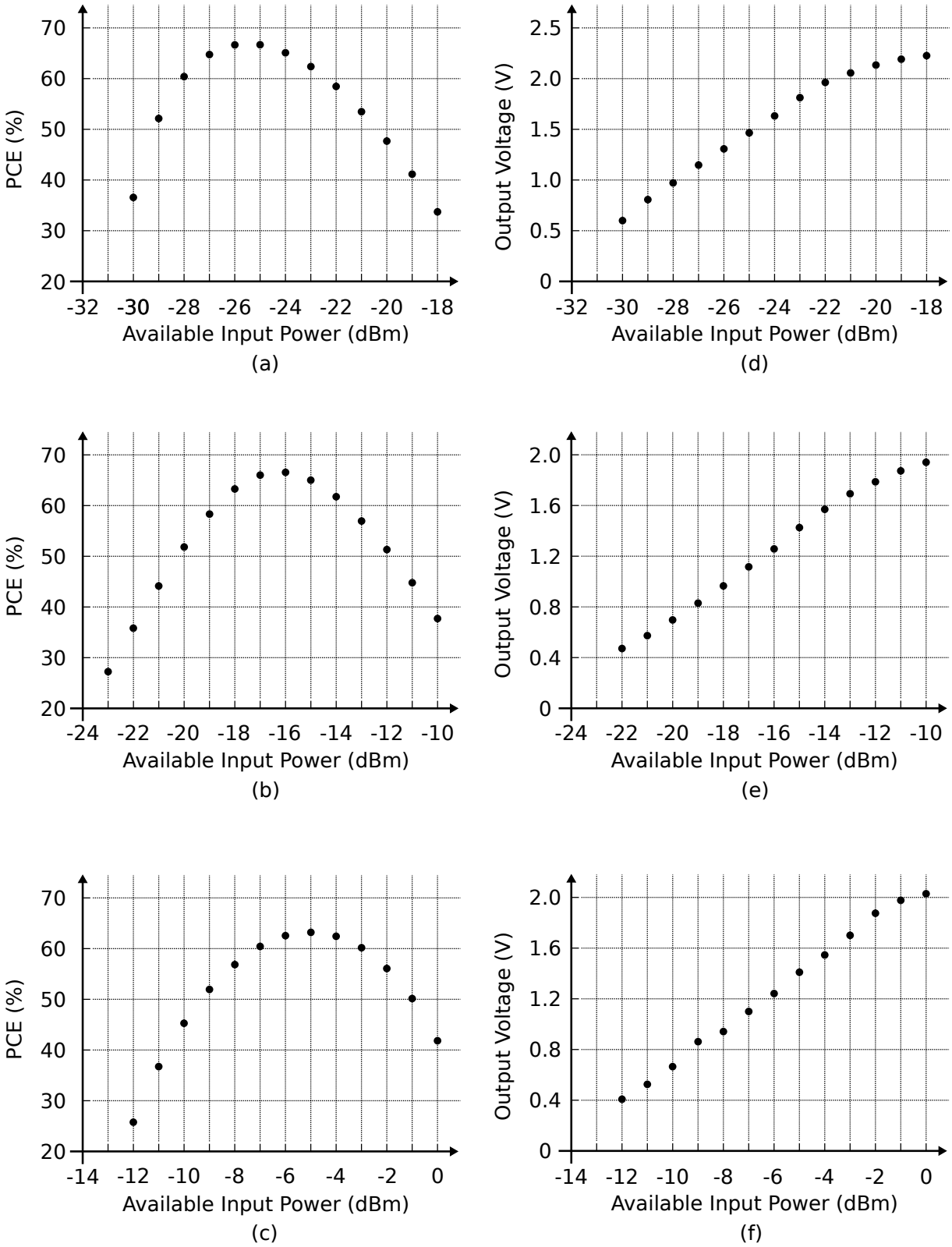


Figure 3.5. PCE vs P_{AVA} and V_{OUT} vs P_{AVA} for a number of loading conditions. PCE vs available input power with a load of (a) 1 MΩ (b) 100 kΩ (c) 10 kΩ and Output voltage vs available input power with a load of (d) 1 MΩ (e) 100 kΩ (f) 10 kΩ

Table 3.1. Performance comparison with prior-art designs (1 MΩ load)

	Process	Frequency	Sensitivity	Max PCE
This Work	130 nm CMOS	915 MHz	−27.6 dBm	66 %
(Hameed et al., 2015)	130 nm CMOS	915 MHz	−20.5 dBm	32 %
(Stoopman et al., 2014)	90 nm CMOS	868 MHz	−23.5 dBm	24 %
(Papotto et al., 2011)	90 nm CMOS	915 MHz	−17.5 dBm	11 %
Theilmann et al. (2012)	250 nm SOS CMOS	915 MHz	−26.4 dBm	N/A
Scorcioni et al. (2013)	130 nm CMOS	868 MHz	−21 dBm	60 %

literature and it can be observed that the proposed design outperforms the other designs presented in the literature in terms of both sensitivity and maximum PCE. In particular, the design achieves higher input power sensitivity than (Theilmann et al., 2012), where specialized near-zero V_{TH} transistors are exploited, interface mismatch is not considered and no reverse-leakage prevention mechanism is implemented.

3.5 Conclusion and Discussion

In this chapter, we proposed a rectifier design for UHF RFID tag chips operating at 915 MHz. With the application of appropriate back-gate biasing into all stages and input matching to the antenna at minimum input power, the PCE of the rectifier reaches maximum near its turn-on threshold. In the post-layout simulation, the proposed rectifier design achieves excellent input power sensitivity and maximum PCE compared with performance figures previously reported in the literature.

From the results, we can also observe the drawback of stand-alone fixed rectifier. Take Figures 3.5 (a) and (d) as an example, as the input power passes -20 dBm, the PCE drops substantially and the output voltage rises above 2 V. From the rectifier side, a lower PCE means that a smaller percentage of the input energy has been delivered from the output. From the load side, having a higher than needed supply voltage means that extra headroom is wasted. Additionally, with three different loading conditions simulated in Figure 3.5, three different optimum source impedance are needed to produce decent PCE figures. However, in a practical application, it is not always possible to frequently change the source impedance. Adaptive and reconfigure rectifier and intelligent power management of the harvested energy are needed to address the fore-mentioned issues, which are covered in Chapter 4, 5 and 6.

Chapter 4

RF Energy Harvester with Peak Power Conversion Efficiency Tracking

RECTIFIER circuits or power harvesters are a critical module in a variety of wireless sensors, radio frequency identification (RFID) tags, and Internet-of-Thing (IoT) devices relying on harvested power from radio waves. Threshold compensation circuit techniques have been proposed in the literature to improve the Power Conversion Efficiency (PCE) of CMOS-based rectifiers. However, these circuits tend to achieve maximum PCE at a specific input power level, and has significantly lower efficiency at other input power levels. In this chapter, we propose a novel energy harvester which maximises its PCE over a wider input power range. The proposed design relies on sensing of the rectifier output voltage, management of the output current and reconfiguration of the rectifier structure. The design, which is implemented in a 130 nm CMOS process, is simulated at 915 MHz. The simulation results show that the harvester is able to develop a 3 V DC at -23 dBm input power while maintaining a PCE above 60% for 20 dB input power range.

4.1 Introduction

In recent years, with the emerging interest in IoTs (Internet of Things), there is an increasing focus on energy harvesting circuits. One very popular branch of these works is energy harvesting from the surrounding EM (electromagnetic) waves. In particular, RF harvesting in the UHF band has been given substantial attention, as a longer power transfer distance can be achieved. As such, rectifiers, as the core of the harvester, has been designed to be efficient at minimum input power, because high sensitivity and long operation range are desired.

Small input power to the rectifier, for a given antenna rectifier interface, means a small input voltage amplitude across the rectifier. When this amplitude becomes so small that it is below the threshold voltage of the transistors used in the rectifier, the rectifier will be unable to convert the input RF to a comparable DC level. Threshold-compensated rectifiers have been demonstrated as the definitive circuit approach to the design of highly sensitive and low-cost CMOS-based rectifiers, and more than a decade of effort has been invested in perfecting this circuit approach (Umeda et al., 2006; Nakamoto et al., 2007; Kotani et al., 2009; Le et al., 2008; Papotto et al., 2011; Hameed et al., 2015) and (Almansouri et al., 2018). With most of these rectifier designs, power conversion efficiency (PCE) tend to peak within a narrow range of input power. However, the PCE is often found to be substantially worse outside this range. Hence, these power harvesting rectifiers are unable to maintain the peak PCE over a wide range of input powers to maximize on available incident energy.

In the context of conventional UHF harvesting system, the main concern for the design of rectifiers is its sensitivity. However, this has been changed with the introduction of hybrid power management unit (HPMU) (Sun et al., 2017,0). In a hybrid system, the excess energy is stored in a capacitor or a rechargeable battery when the harvester system is close to the power source. The stored energy can then be used when the system is moving away from the transmitter where the harvested power is insufficient to supply the system operation. Because the excess power can be stored for later use, it is more desirable that the rectifier is efficient at all input power levels.

Notably, maximum power efficiency tracking was explored in (Dolgov et al., 2010; Dehghani et al., 2016; Choi et al., 2016). Dolgov et al. (2010) requires an external micro-controller and Dehghani et al. (2016) operates with milliwatt-level input power, thus both of them are unsuitable for ultra-low power energy harvesting. In Choi et al.

(2016), efficiency tracking scheme is developed for low frequency rectifier (i.e. 50 kHz), thus it is ill-suited to energy harvesting in the UHF band.

In this chapter, a reconfigurable UHF energy harvester is proposed. The design achieves excellent PCE across a wide input power range while maintaining competitive input power sensitivity. The proposed design is unique in that it tracks the maximum power efficiency by exploiting the relationship between the input voltage, output voltage and the PCE, resulting in an efficient and compact analog solution. In the rest of the chapter, the limitations of threshold-compensated rectifiers are first described in Section 4.2. Then, the proposed peak PCE tracking technique is introduced in Section 4.3. Proposed design and simulation results are presented in Sections 4.4 and 4.5, respectively. Finally, a summary and conclusion are presented in Section 4.6.

4.2 Limitation in Existing Threshold Compensated Rectifiers

Previous studies such as (Papotto et al., 2011) and (Kotani et al., 2009) have demonstrated the tight trade-off between forward conduction and reverse leakage, preventing the rectifier from achieving high PCE over a wide range of input power. For most threshold-compensated rectifiers, the PCE is insignificant at very low input power, this is because the input power is too small to turn on the diode within the rectifier. With threshold compensation, the diode starts to turn on earlier than without. Thus, initially, as the input power increases, the forward conduction capability of the diodes improves and subsequently the PCE of the rectifier improves. However, as the input power increases, the output voltage of the rectifier also increases; as the output voltage builds up and the threshold compensation continues to occur, the reverse leakage becomes significant and starts to dominate over the forward conduction and, subsequently, the PCE starts to decrease. Therefore, the peak PCE occurs when a good trade-off between the forward conduction and reverse leakage can be obtained as shown in Figure 4.1.

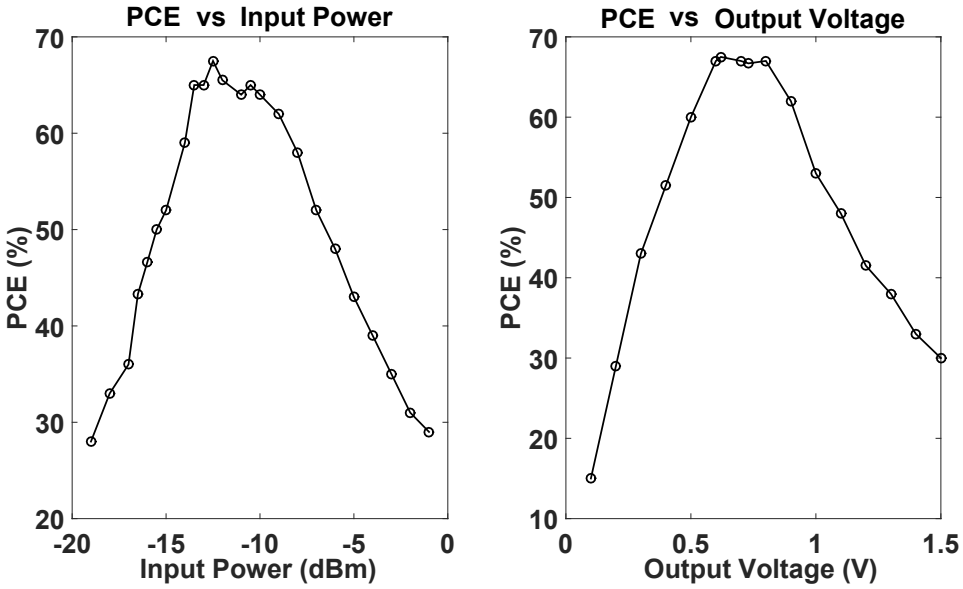


Figure 4.1. Peaking behaviour in PCE in terms of input power and output voltage. Reproduced from the single stage differential-drive rectifier proposed in (Kotani et al., 2009).

4.3 Peak PCE Tracking Technique

From Figure 4.1, we observe that if the output is regulated to the voltage where maximum PCE is achieved, the PCE can be optimized over a wide range of input power. One way to regulate the output voltage is to drain the output current while the input power increases. This increase in input power and subsequently an increase in the output voltage is counter-reacted by an increase in the drained current from the output of the rectifier. Similarly, if the input power is decreased, the drained current will be decreased, maintaining the output voltage at a pre-set voltage. This concept is depicted in Figure 4.2 (a).

4.3.1 Quantitative Analysis

To verify this, a 130 nm CMOS process was used for the following simulations, using the simulation set-up shown in Figure 4.2 (b). The rectifier circuit topology used in Figure 4.2 (b) is a 3-stage differential-drive CMOS rectifier (Kotani et al., 2009), which is shown in Figure 4.2 (c). In these simulations, the input power is swept from 10 μW up to 800 μW, while the current drawn from the rectifier output was set to 5 μA, 10 μA, 20 μA, 50 μA, 70 μA, 100 μA, 120 μA, and 150 μA at an operating frequency of 915 MHz. The simulated PCE as a function of input power and current is shown in Figure 4.3 (a). In addition, the relationship between the output voltage and the PCE is plotted

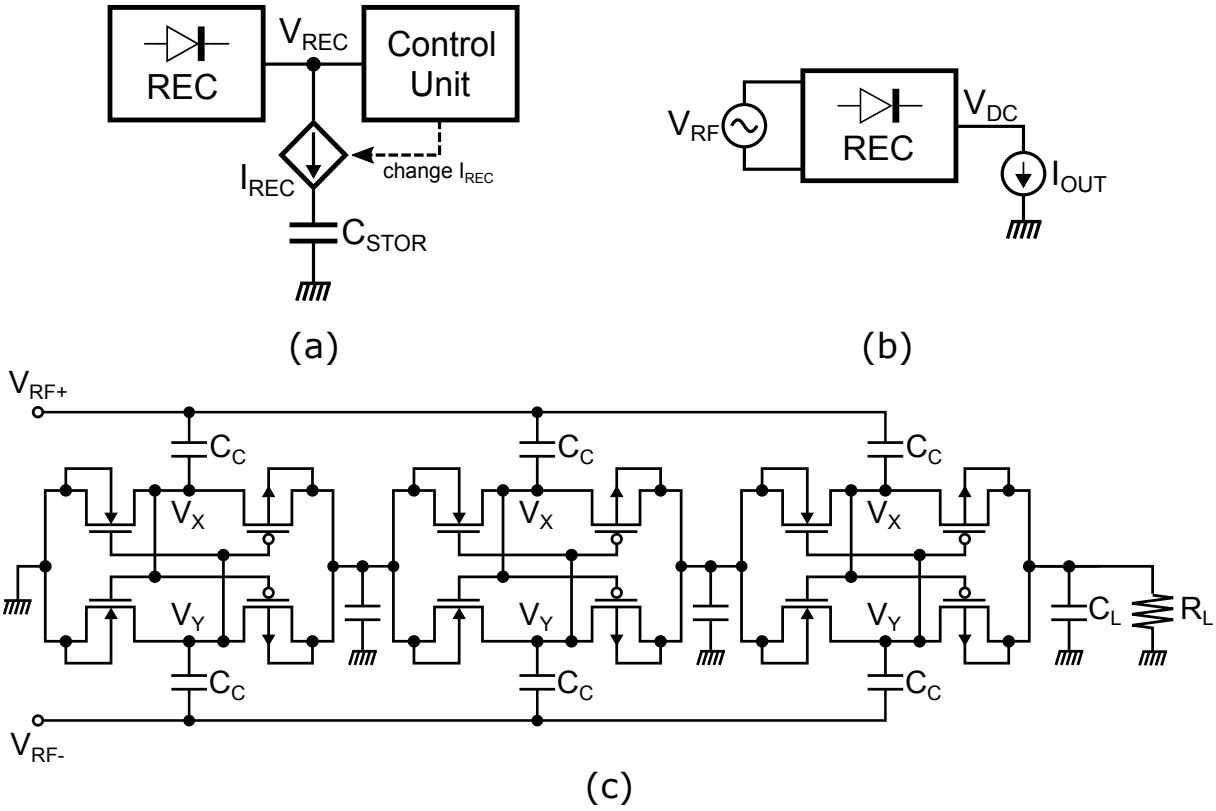


Figure 4.2. The peak PCE tracking idea. (a) A diagram of the proposed idea, where the control unit regulates the output voltage of the rectifier V_{REC} by changing the output current of the rectifier I_{REC} (b) The simulation set-up used to generate the simulation results shown in Figs. 4.3 (a) & (b); (c) The 3-stage differential-drive rectifier schematic used in simulation

in Figure 4.3 (b). Interestingly, as can be observed in Figure 4.3 (b), the relationship between the output voltage and PCE shifts to a higher voltage as the output current increases and to a lower voltage as the output current decreases. Consequently, the PCE optimal voltage is a function of the output current. As the output voltage is regulated by changing the current drained from the output of the rectifier, the input power to the rectifier determines the output current and subsequently the optimal voltage at a specific PCE. Specifically, as input power increases, the optimal output voltage increases and the output voltage vs PCE curves shifts to a higher voltage. Conversely, as the input power decreases, the optimal voltage decreases and the output voltage vs PCE curves shifts to a lower voltage. Hence, as the input power changes, the optimal PCE cannot be achieved with the output regulated to a specific voltage.

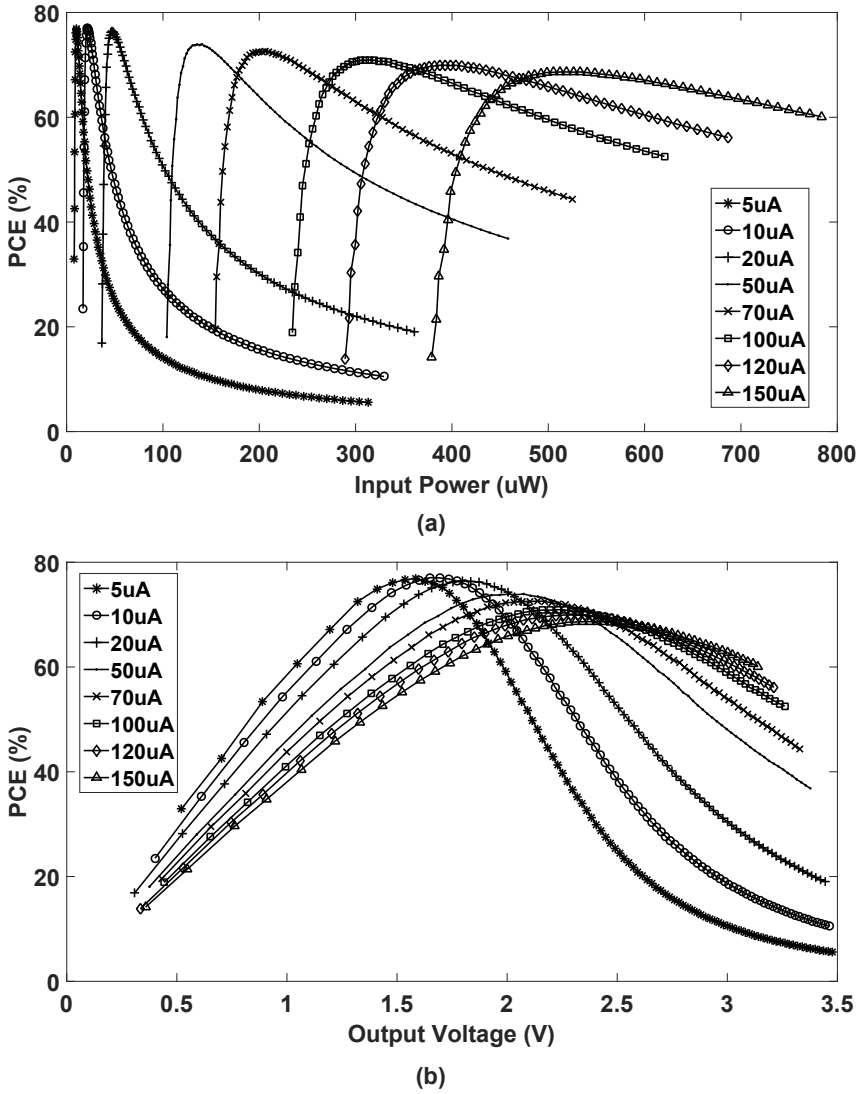


Figure 4.3. Simulation results of the quantitative analysis. (a) Input power vs PCE of the 3-stage differential-drive rectifier (b) Output voltage vs PCE of the simulated 3-stage differential-drive rectifier

4.3.2 Proposed Concept

There are two approaches to address this problem. In the first approach, we regulate the output voltage by changing the output current. When the input power increases, the optimal output voltage increases. We reduce the number of stages in the rectifier chain to increase the effective output voltage per stage. Hence, the PCE optimal output voltage of the whole rectifier is effectively decreased, effectively compensating the rising PCE optimal output voltage. This curve shifting process is depicted in Figure 4.4 (a) and conceptual diagram is illustrated in Figure 4.4 (b).

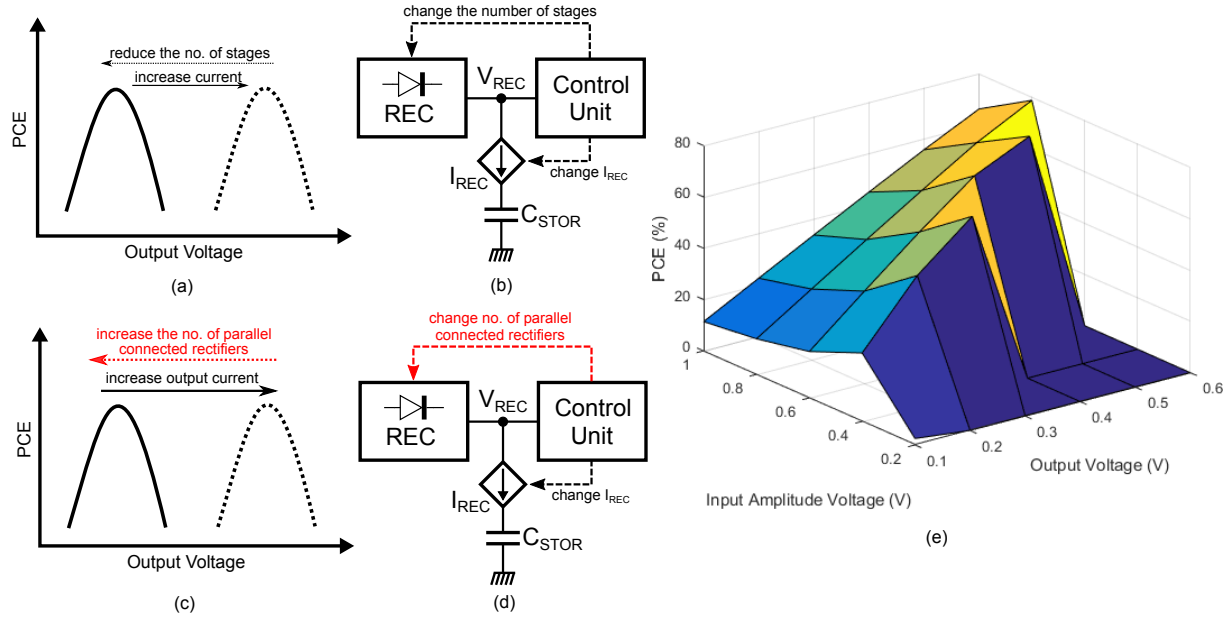


Figure 4.4. The curve shifting concept. (a) Illustration of the first curve shifting strategy (b) Conceptual model of the first curve shifting strategy, where the control unit regulates the output voltage of the rectifier V_{REC} by changing the output current of the rectifier I_{REC} and it also reconfigures the number of stages within the rectifier as a function of input power (c) Illustration of the second (better) curve shifting strategy (d) Conceptual model of the second (better) curve shifting strategy, where the control unit regulates the output voltage of the rectifier V_{REC} by changing the output current of the rectifier I_{REC} and it also reconfigures the number of parallel-connected rectifiers as a function of input power (e) PCE of a single stage differential cross-coupled rectifier as the input amplitude and output voltage vary

However, the root cause for the shifting in this PCE optimal output voltage and the reduction in peak values, is that the intrinsic PCE is also dependent upon the input RF voltage amplitude as well as the output DC voltage. As the input power increases, for the same rectifier loaded at the RF input, the input RF voltage amplitude increases, degrading the PCE of the rectifier. A 3-D plot of the intrinsic PCE dependency of the rectifier in terms of both input (RF) amplitude and output DC voltage is depicted in the Figure 4.4 (e). The second approach can therefore be described as follows. As can be observed from Figure 4.3 (b), if the output voltage is regulated to the PCE optimal output voltage for a particular load current, as the load current increases and the output voltage vs PCE shifts to the right, the PCE will no longer be optimal. If more rectifier stages are loaded across the RF input and are used to produce the final DC output, we are able to reduce the input amplitude and effectively shift the output

vs PCE curve back to where it was, with no degradation in peak PCE. This process is illustrated in Figure 4.4 (c). The concept model of the design that implements this proposed curve shifting is shown in Figure 4.4 (d).

4.3.3 Dynamic Reverse Leakage

Another merit of the proposed design is the prevention of dynamic reverse leakage. This is not to be confused with the reverse leakage discussed previously, which occurs in steady state. In systems where the rectifier is directly connected to the storage capacitor, in the event of a sudden drop in input power, the charge already stored on the capacitor will potentially flow out of the capacitor and back into the rectifier. A classical solution to this problem is to design the last stage of the rectifier with diode-connected transistors (Papotto et al., 2011) at the expense of lower power efficiency and sensitivity. In this design, as shown in Figure 4.4 (d), the storage capacitor is shielded from the rectifier, preventing the stored charge from flowing back into the rectifier. When the input power drops, the control unit reduces I_{REC} so that V_{REC} stays at the pre-set voltage. With this approach, the reverse leakage is suppressed without sacrificing the overall power efficiency or sensitivity.

4.4 Proposed Reconfigurable Rectifier Design

From our previous discussion, to maintain the input amplitude of the rectifier at roughly the same level over a wide range of input power, while still maintaining a good intrinsic PCE is to have the rectifier reconfigured based on the input power level, such configuration can vary from having 1 6-stage to 6 6-stages in parallel. However, the rectifier-antenna interface efficiency, due to matching, plays an important role in the overall conversion efficiency. It is therefore studied extensively in Section 4.4.1.

4.4.1 The Study of Interface Efficiency

The input impedance of the rectifier consists of a real part and an imaginary part. To investigate the effect of input impedance variation on the rectifier PCE, we need to look at the effect of the real part and imaginary parts individually. Firstly, we need to study the input impedance variation only due to the increase in input power, and

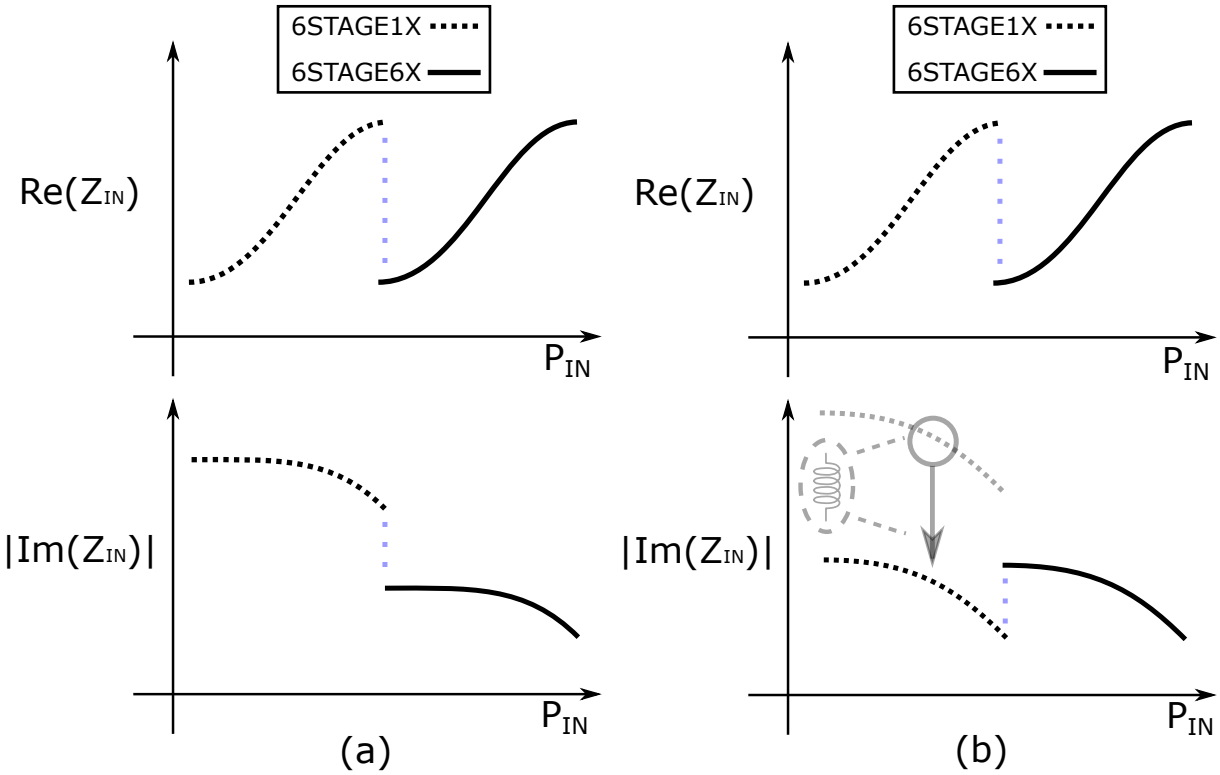


Figure 4.5. The study of interface efficiency. (a) Real (desirable) and Imaginary (undesirable) parts of the input impedance of the 1X and 6X rectifier (b) Real (desirable) and Imaginary (desirable) parts of the input impedance of the 1X and 6X rectifier, modified by the serially connected inductors

effectively, the increase in amplitude. Secondly, we need to study the variation of input impedance due to the rectifier reconfiguration. As the input power increases, the ohmic losses, hence the real part naturally increases and the capacitance decreases as a result of it.

For the real part impedance, the reconfiguration from one 6-stage to 6 6-stages in parallel results in reduction because more rectifier stages are loaded across the RF input. On the other hand, the capacitance will increase due to the increase in the number of loaded rectifiers, this results in reduction in the imaginary part of the input impedance. The change in the real and imaginary part of the input impedance as a result of the change of input power and the rectifier reconfiguration is depicted in Figure 4.5 (a).

The principal design goal of the harvester is to achieve consistently high PCE over a wide range of input power, it is therefore desirable to the maintain the real and imaginary parts of the input impedance at a relatively fixed value over the operational

input power range so that the antenna can be designed to conjugately match to this impedance to achieve high interface efficiency. As can be observed in Figure 4.5 (a), while the reconfiguration (from 1 6-stage to 6 6-stages) compensates the rising real part of the input impedance, it worsens the imaginary part of the input impedance, increasing its variation over the entire input power operational range. Thus, if we design the antenna to be matched at an input power level in the low power mode, the interface will be heavily mismatched in the high input power mode. On the other hand, if we design the antenna impedance to be matched at an input power level in the high-power mode, the interface will be heavily mismatched in the low input power mode. To mitigate this, in the low power mode, we add two inductors in series to the input of the rectifier, to partially tune out the negative reactance of the rectifier's input. Then, in the high input power mode, we switch out the inductor to compensate for the reduction in reactance due to switching from 1X to 6X rectifier configuration. The resulted input impedance characteristics over a wide range of input power is as shown in Figure 4.5 (b) and both the real and imaginary parts of the input impedance fluctuates around a fixed value, reducing the total variation of the imaginary part over the entire operational input power range.

4.4.2 Intelligent Switch Design

To physically realise the aforementioned reconfiguration, switching stages in and out on the RF input path are necessary. Conventionally, a RF switch is employed to switch in and out the main rectifier stages (Masuch et al., 2013), as shown in the Figure 4.6 (a). However, the design of RF switch presents a tight trade-off between the isolation and insertion loss and also introduces passive parasitics, these combined result in very poor overall system efficiency in low input power range (i.e. less than -10 dBm).

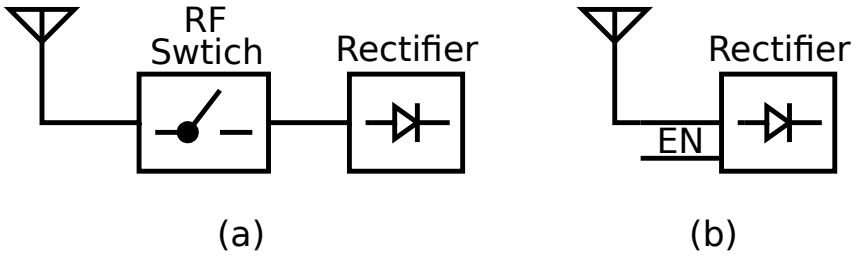


Figure 4.6. (a) The conventional switching scheme (b) Rectifier with a disable mode.

Due to this reason, rather than turning off the rectifier with a switch, in this work, we propose a new scheme where we enable and disable the rectifier, depicted in Figure 4.6

(b). To understand how this can be done, we need to re-visit the operational principle of the differential cross-coupled rectifier. The schematic of the classical differential cross-coupled rectifier is shown in Figure 4.7. The common mode voltage of the output of phase V_X and V_Y provides threshold compensation, resulting in higher efficiency for small input voltage amplitude and subsequently low input power.

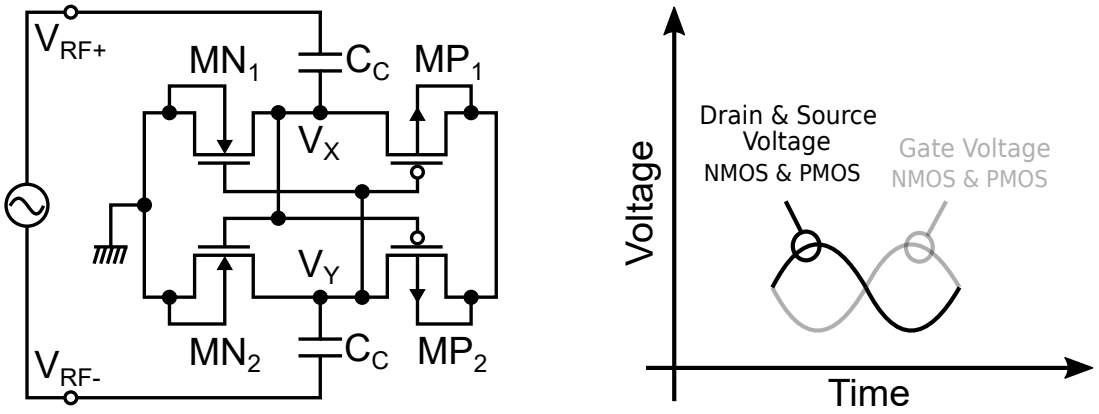


Figure 4.7. The voltage waveform of the classical cross-coupled differential rectifier.

Potentially, we could turn off this rectifier by reducing the DC level of the NMOS gate voltage while increasing the DC level of the PMOS gate voltage, as illustrated in Figure 4.8. This is because the down-shifted and up-shifted gate voltages cause both NMOS and PMOS transistors to remain off for the entire RF input cycle, thus the RF input appears to be an open circuit. This approach is superior in that we are disabling the rectifier rather than blocking the RF input, eliminating the tight trade off between the insertion loss and isolation of an RF switch. In addition, this approach also minimizes the input parasitic capacitance which would be otherwise introduced by the RF switch.

To realize this approach at the circuit level, auxiliary rectifier stages (REC_{11}, REC_{12}, REC_{21}, REC_{22}) are used to shift the DC level of the gate voltages of NMOS and PMOS relative to their source and drain voltages. As illustrated in Figure 4.9, in the "ON" state of the main rectifier, REC_{12} and REC_{22} are configured to be in parallel with the main rectifier, leaving the DC level of the gate voltages of the NMOS and PMOS unshifted. In the "OFF" state of the main rectifier, as shown in Figure 4.9, the auxiliary rectifier REC_{11} and REC_{12}, REC_{21} and REC_{22} are configured in series, respectively. As such, the DC level of the NMOS gate voltage are down-shifted whereas the DC level of the PMOS gate voltage are up-shifted, effectively turning off the main rectifier.

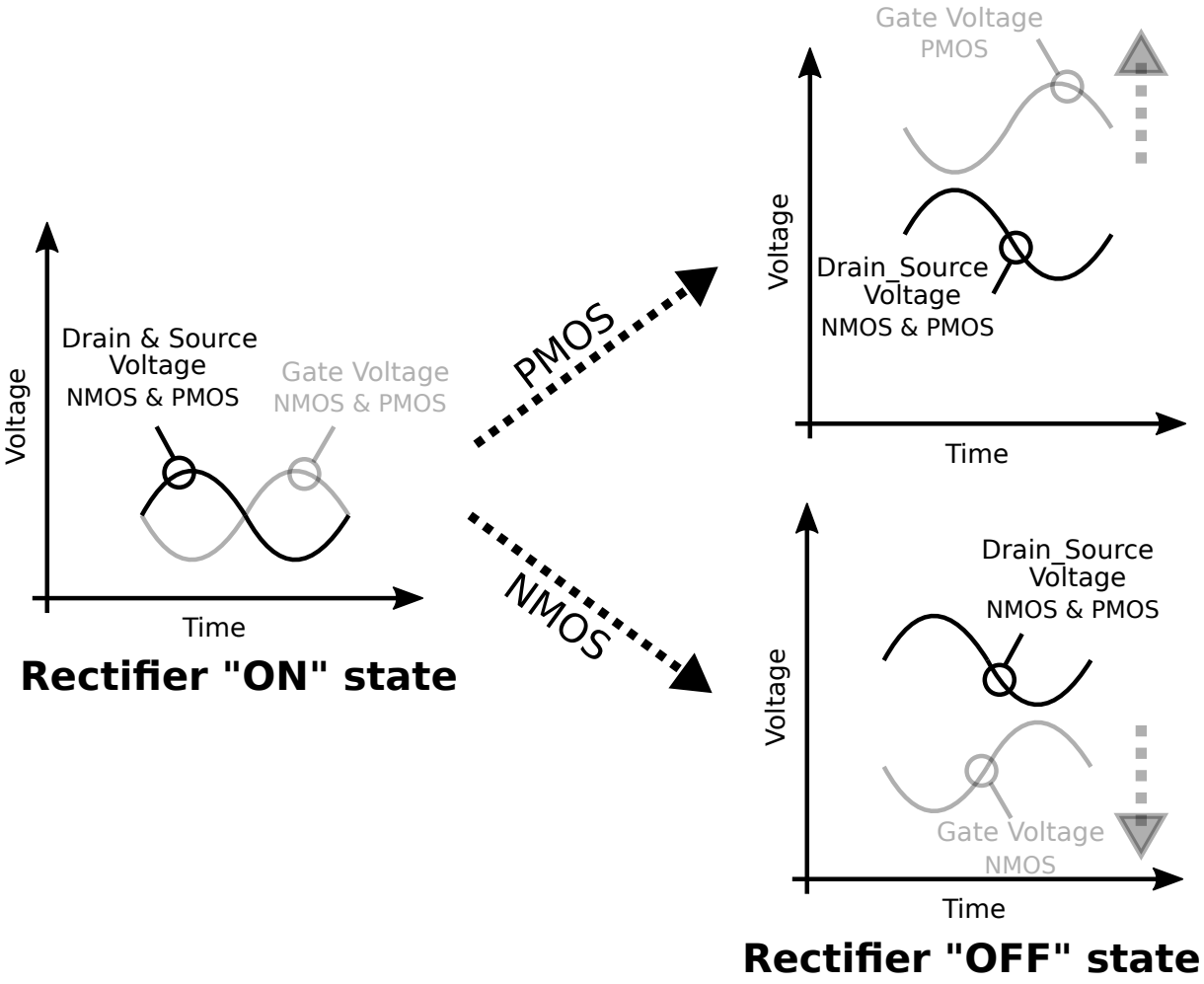


Figure 4.8. The rectifier switch action.

The above-mentioned rectifier reconfiguration is realized through the implementation of switches as shown in Figure 4.10. To ensure reliable isolation in the "OFF" state of the switch, it is implemented as a pair of serially connected NMOS and PMOS transistors. In the "ON" state of this reconfigurable rectifier, the switches S_{11}, S_{13}, S_{21} and S_{23} are closed, whereas switches S_{12} and S_{22} are open. As such, the auxiliary REC_{12} and REC_{22} are configured to be in parallel with the main rectifier, and the auxiliary REC_{11} and REC_{21} are floating. In the "OFF" state of this reconfigurable rectifier, the switches S_{11}, S_{13}, S_{21} and S_{23} are open, whereas switches S_{12} and S_{22} are closed. As such, the auxiliary rectifiers REC_{11} and REC_{12}, REC_{21} and REC_{22} are configured in series, respectively. The switch setting is summarized in the Table 4.1.

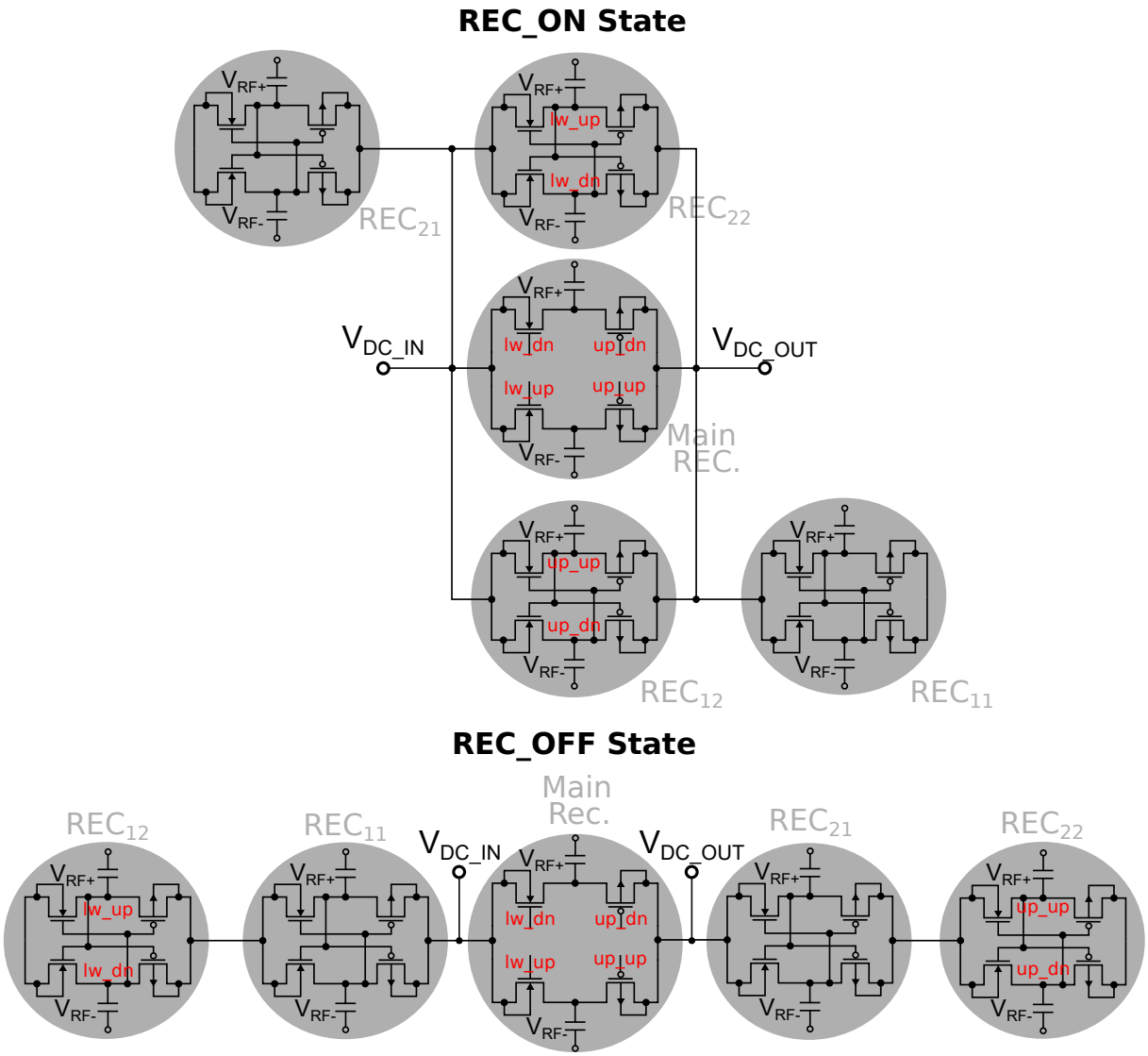


Figure 4.9. The rectifier configuration in the REC_ON and REC_OFF state, respectively.

4.4.3 Start-up Mechanism

For an energy harvester, at system start-up, no DC voltage can be developed at the output. Thus, initially, we don't have the supply voltage to turn on the switches in the 1X main rectifier, thus the whole harvester is not able to start properly. To mitigate this problem, an auxiliary rectifier is added to provide the supply voltage to turn-on the reconfiguration switches as depicted in Figure 4.11. Specifically, a 6-stage auxiliary rectifier was designed to develop the initial V_{OUT} needed to turn on the reconfiguration switches of the main rectifier. This approach allows the DC level of the output voltage of both the main and the auxiliary rectifiers to be well defined, significantly improving

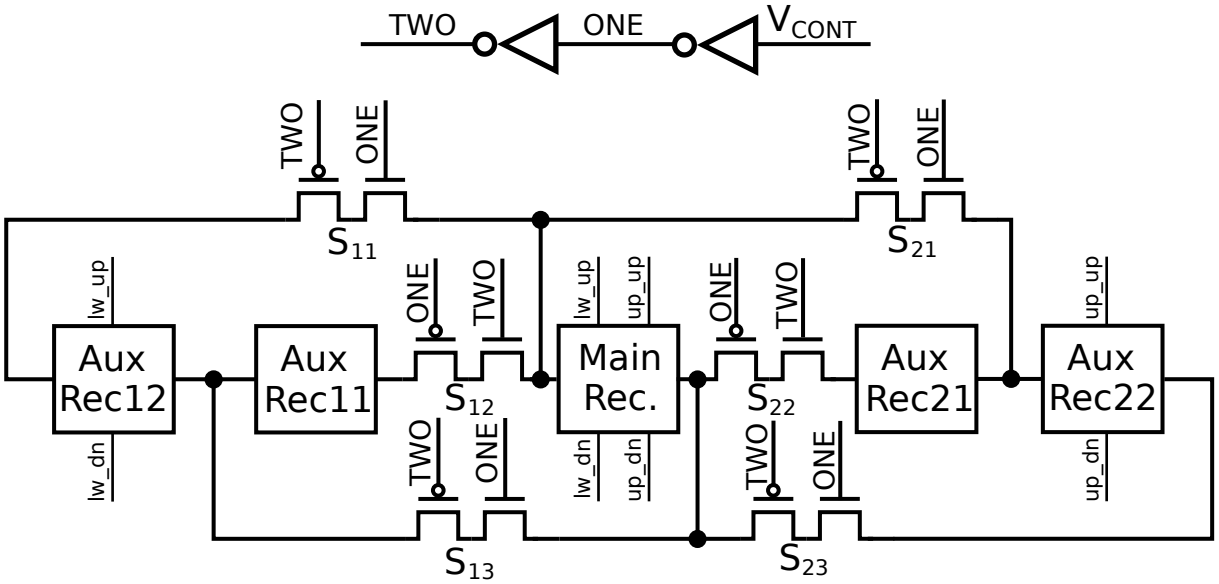


Figure 4.10. The proposed reconfigurable rectifier to avoid the use of RF switches.

Table 4.1. Rectifier Switch Setting Table

REC MODE	S_{11}	S_{12}	S_{13}	S_{21}	S_{22}	S_{23}
REC OFF	ON	OFF	ON	ON	OFF	ON
REC ON	OFF	ON	OFF	OFF	ON	OFF

the reliability of the reconfiguration switching scheme. In addition, we pass the output current of the auxiliary stage to the V_{OUT} regulation block as well, thus no charge is wasted.

A control pin, V_{CONT}, from the V_{OUT} regulation block is used as the control signal to turn on or off the main rectifier. The logical high level of this control signal is V_{OUT} while its logical low level is ground. Naturally, we will encounter the following problems when we are doing the switching. For earlier stages (e.g. the 1st stage), the turn-on voltage for the NMOS switches (i.e. S_{12}, S_{21} and S_{23}) are strong, but turn off voltage for the NMOS switches are weak. On the other hand, turn-on voltage for the PMOS switches are weak but the turn-off voltage for the PMOS switches are strong. For the latter stages (e.g. the 6th stage), the turn-on voltage for the NMOS switches (i.e. S_{12}, S_{21} and S_{23}) are weak, but turn off voltage for the NMOS switches are strong. On the other hand, turn-on voltage for the PMOS switches are strong but the turn-off voltage for the PMOS switches are weak.

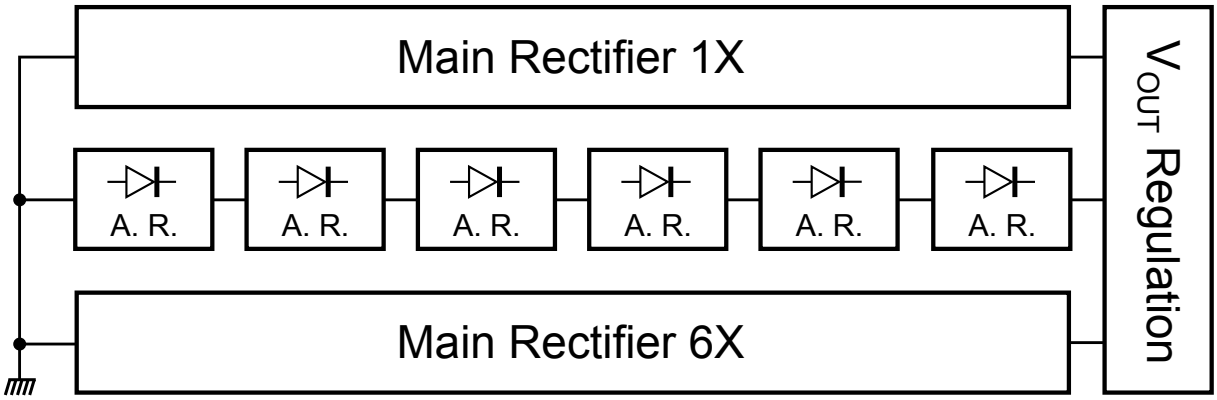


Figure 4.11. The diagram that illustrates the start-up rectifier.

One way to mitigate these issues, is to create an auxiliary control circuitry and rectifier stages, which is able to increase the voltage level of the logical high signal and to reduce the voltage level of the logical low signal. However, this approach unnecessarily overdrives the gate of a few FET switches and overcomplicates the circuitry. In this work, we exploit multi-Vth devices available in our process and use them to solve this problem. The device choices and rationales for using them are summarized as follows:

- For stages 1 to 2, a nominal transistor (V_{TH} = 0.7 V) for the NMOS switch and a native transistor (V_{TH} = 0 V) for the PMOS switch can be used. In the OFF mode, the high V_{TH} in NMOS and the large reverse V_{SG} provides the isolation. In the ON mode, the large positive V_{GS} and zero-threshold in the PMOS provides conduction.

- For stages 3 to 4, a V_{TH} transistor (V_{TH} = 0.3 V) for the NMOS switch and also a low V_{TH} transistors (V_{TH} = 0.3 V) for the PMOS switch can be used. In these two stages, the turn on voltage (positive V_{GS}) and the turn-off voltage (negative V_{GS}) are both adequate, thus any transistor with reasonable threshold would suffice here.

- For stages 5 to 6, a native transistor (V_{TH} = 0 V) for the NMOS switch and also a nominal V_{TH} transistor (V_{TH} = 0.7 V) for the PMOS switch. In the OFF mode, the large reverse V_{GS} in NMOS and high V_{TH} provides good isolation. In the ON mode, the zero threshold voltage in the NMOS and the large positive V_{SG} turn on voltage provides sufficient conduction.

It needs to be noted that, in a device limited process, it would be sufficient to just use two types of devices. For example, for 1 to 3 stages, a nominal V_{TH} transistor for the NMOS and a native transistor for the PMOS can be used. For stages 4 to 6, a native V_{TH} transistor for the NMOS and nominal V_{TH} transistor for the PMOS can be used.

4.4.4 System-level Implementation and the Implementation of the regulator circuit

The system-level block diagram is shown in Figure 4.12. It can be observed that the two 20 nH inductors are connected to 1X rectifier (in the low power mode) and the 6X rectifier (in the high power mode) is connected to the antenna directly through bonding wires.

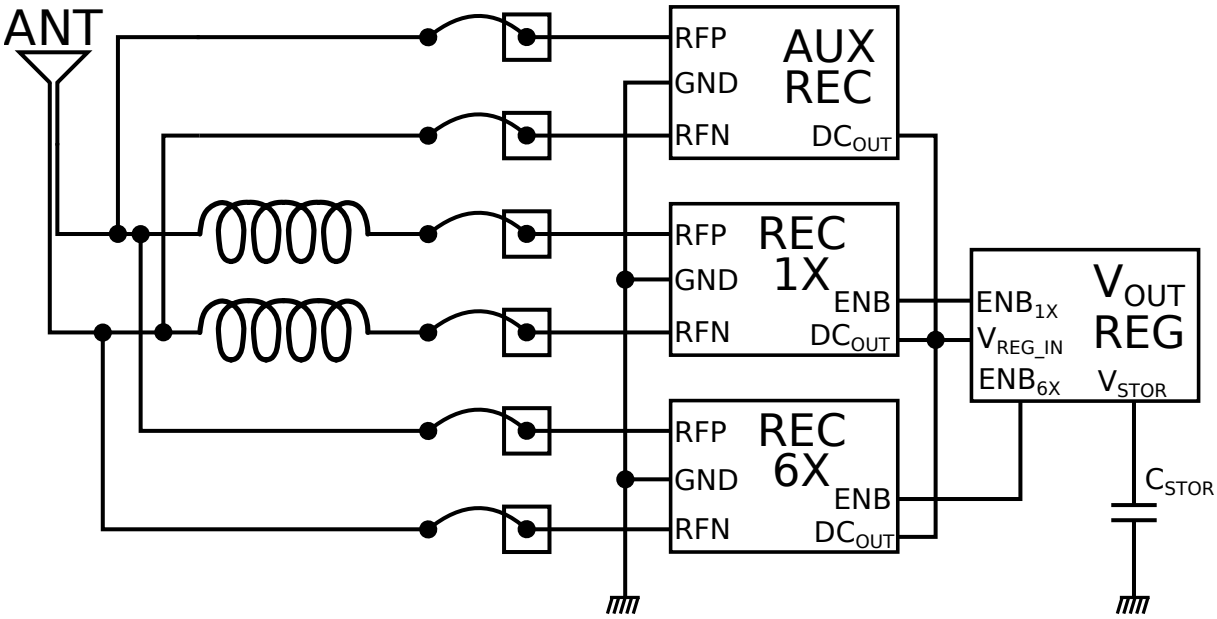


Figure 4.12. The top level schematic of the proposed harvester.

The V_{OUT} regulation module is depicted in Figure 4.13. As discussed in the previous section, the auxiliary rectifier starts up and charges the intermediate storage capacitor C_{OUT}, because it does not have reconfiguration mechanism and is hard-wired for continuous operation. During this start-up process, the state of the reconfiguration switches are undefined. To prevent the charges pumped through the auxiliary rectifier from being leaked through the main rectifier and not having any voltage developed at V_{OUT} by the auxiliary, a PMOS switch MP_{SW} is added between V_{OUT} and the output

of main rectifier. The added switch is then controlled by the voltage detector VDET via V_{PSW}. After the V_{OUT} is developed by the start-up auxiliary rectifier and the reconfiguration switch voltages for the main rectifiers are ready, the voltage detector VDET turns on the switch MP_{SW} so that the charge pumped through the main rectifiers are also directed to the V_{OUT} regulator.

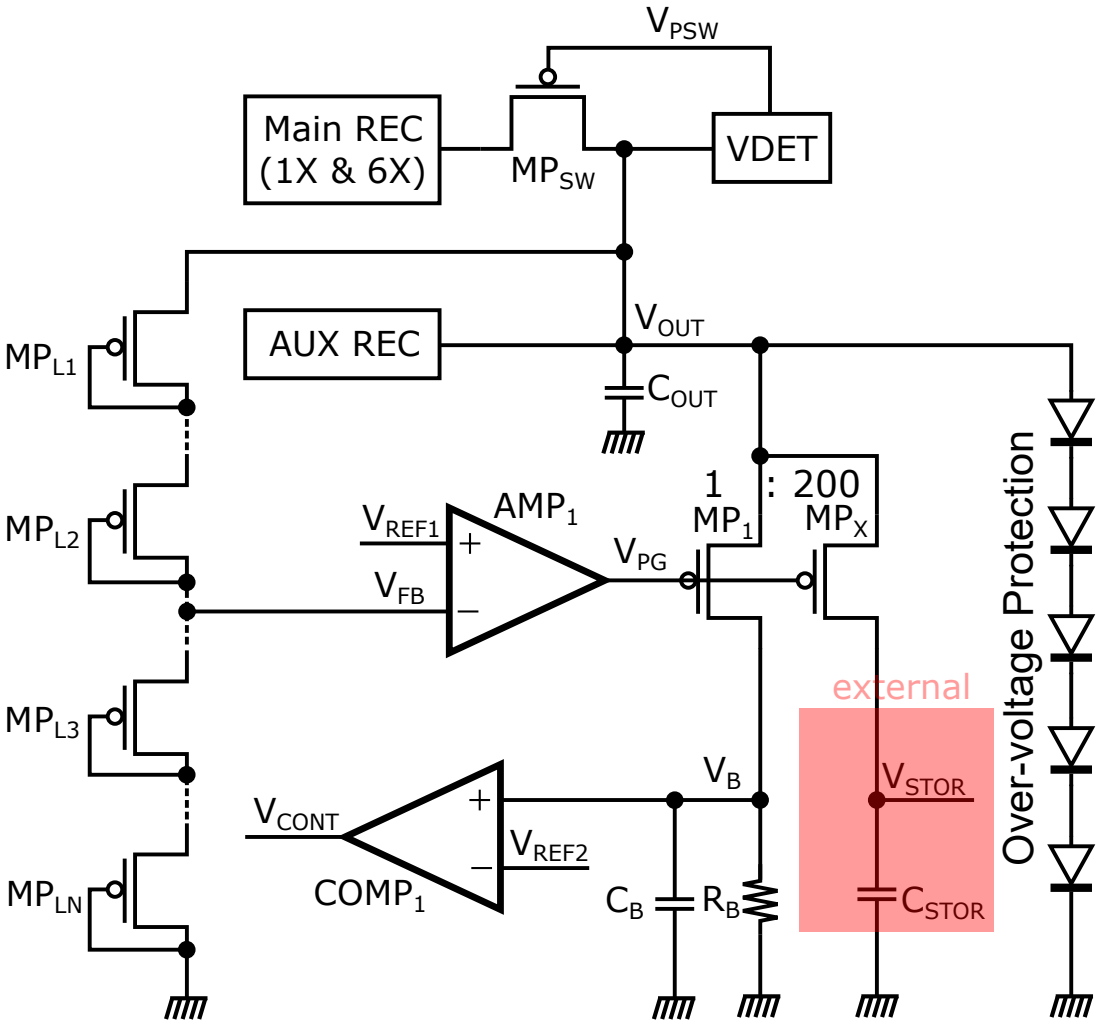


Figure 4.13. Circuit realization of the proposed output regulation circuit.

The core of the V_{OUT} regulation circuitry consists of an amplifier AMP_1, a wide PMOS MP_X for power delivery and diode-connected PMOS voltage divider ladder MP_{L1} through to MP_{LN}, which together forms the main regulation loop. In addition to this, a decision making circuitry that instructs the harvester to reconfigure from 1 6-stage into 6 6-stage rectifiers (and vice versa) is also included and it consists of a comparator $COMP_1$ and a much smaller PMOS transistor MP_1.

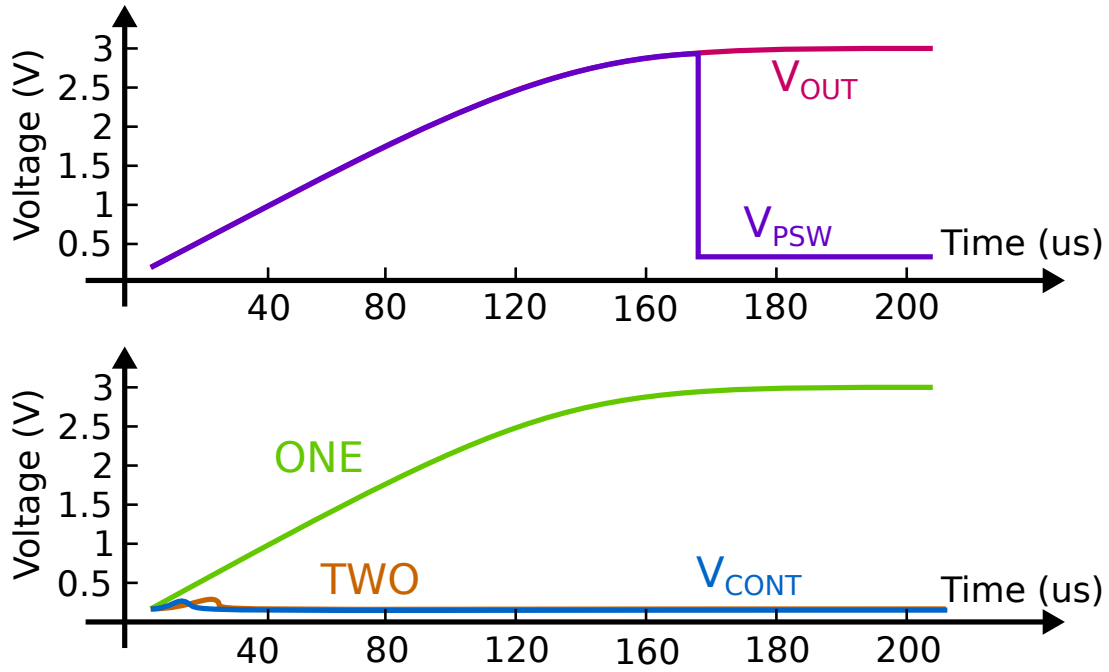


Figure 4.14. Simulated start-up transient of the harvester system. Note that the signal ONE and TWO can be found in the reconfigurable rectifier shown in Figure 4.10 and the signal V_{CONT} can be found in the output regulation circuitry shown in Figure 4.13.

The operation principle of the V_{OUT} regulator is as follows: AMP_1, MP_X and the voltage divider realized by a string of diode-connected PMOS transistors regulates the V_{OUT} to 3 V by changing the current drained from the output of the rectifier through MP_X and all the current is directed into the capacitor C_{STOR} for storage. The width of MP_1 is 1/200 of MP_X, thus only a tiny slice of the current passes through MP_X and resistor R_B. When the output current increases, V_B rises and when it becomes greater than V_{REF2}, $COMP_1$ pulls up its output, V_{CONT}. V_{CONT} can then be used to derive the needed digital signals (e.g. ONE and TWO) in reconfigurable rectifier, as shown in Figure 4.10.

4.5 Simulation Results

Both the post-layout transient and steady-state performance of the harvester are thoroughly investigated. Then, to consider the circuit reliability, the effect of process variation on power conversion efficient of the harvester is studied.

4.5.1 Transient Behaviour

For a reconfigurable rectifier, the start-up process is the most critical aspect from a stability standpoint. This is because, in the initial start-up phase, supply voltage for the reconfiguration switches are not yet ready and hence its behaviour is somewhat undefined. Thus, the start-up behaviour needs to be thoroughly investigated.

As discussed in the previous section, the PMOS switch MP_{SW} is added to prevent reverse leakage back into the main rectifier in cases where the switches in the 1X main rectifier are not ON at start-up. In extremely rare cases where the reconfiguration switches are ON at start-up, possibly due to residual charges in capacitors, the PMOS MP_{SW} does not function as an open switch. Instead, the main rectifier will charge the temporary capacitor C_{OUT} through the diode-connected MP_{SW} together with the auxiliary rectifier. When the V_{OUT} reaches the threshold, the voltage detector VDET pulls down the gate terminal of MP_{SW}, main rectifier is connected to V_{OUT} regulator and normal operation resumes thereafter. Hence, the PMOS switch together with the auxiliary rectifier provides a reliable start-up for the harvester system.

The start up transient is simulated and key waveforms are shown in Figure 4.14. The start-up auxiliary rectifier first starts up and charges the on-chip capacitor C_{OUT} and V_{SW} is pulled down to engage the main rectifier when V_{OUT} rises to close to 3 V. When this happens, the node voltages (i.e. ONE and TWO) for the reconfiguration switches are already in place, thus the start-up process is successful and normal system operation resumes.

4.5.2 Steady-state Behaviour

The steady state performance of the proposed harvester design has been simulated at 915 MHz at various different input power levels, being driven from a source impedance of $23 + j490\ \Omega$ for best matching when simulating in the typical corner. All steady state simulations are conducted in PSS HB engine in Cadence Virtuoso. In this work, we have used the following three metrics to demonstrate the performance of our design, (1) the intrinsic PCE of the rectifier (PCE) (2) the interface efficiency (IFE) (3) end-to-end efficiency of the whole harvester (EEE). These are plotted

in Figures 4.15, 4.16 and 4.17, respectively. In addition, they are defined in Equations 4.1 4.2 and 4.3, respectively.

$$\text{PCE} = \frac{\text{P}_{\text{OUT}}}{\text{P}_{\text{IN}}} \tag{4.1}$$

$$\text{IFE} = \frac{\text{P}_{\text{IN}}}{\text{P}_{\text{AVA}}} \tag{4.2}$$

$$\text{EEE} = \frac{\text{P}_{\text{OUT}}}{\text{P}_{\text{AVA}}} \tag{4.3}$$

where P_{IN} and P_{OUT} are the measured input and output power, respectively, after the system reaches steady state, P_{AVA} is the available power from the source. There isn't a large number of designs which attempt to maintain high PCE across a wide input power range, as the motivation for this was not clear until the hybrid power management unit (Sun et al., 2017). A prior-art design (Scorcioni et al., 2012) which also attempts to achieve high PCE over a wide input power range and two other start-of-the-art designs Stoopman et al. (2014); Scorcioni et al. (2012); Hameed et al. (2015); Almansouri et al. (2018); Kotani et al. (2009) are included in Table 5.2.

4.5.3 Effect of Process Variation

In the literature of UHF energy harvesting, the effect of process variation is rarely discussed. However, for a practical design to be qualified for production, it is often useful to study and understand how robust the performance is in the presence of process variation and mismatch. In this work, there are two important performance metrics and they are the peak efficiency and the bandwidth of high efficiency (e.g. $>$60%).

We conducted both global MC (for randomly generated process corners) and local MC (for randomly generated mismatched device parameters) simulations to verify the two above-mentioned performance metric and a total of 1000 sampled MC simulations were run. In the simulation setting, a special device model is used to enable the generation of the statistical variations of both local mismatch and global process. The results of peak efficiency and high efficiency bandwidth are shown in Figure 4.18. As can be observed, the design performs excellently in both metrics under the influence of both global process variations and local mismatch.

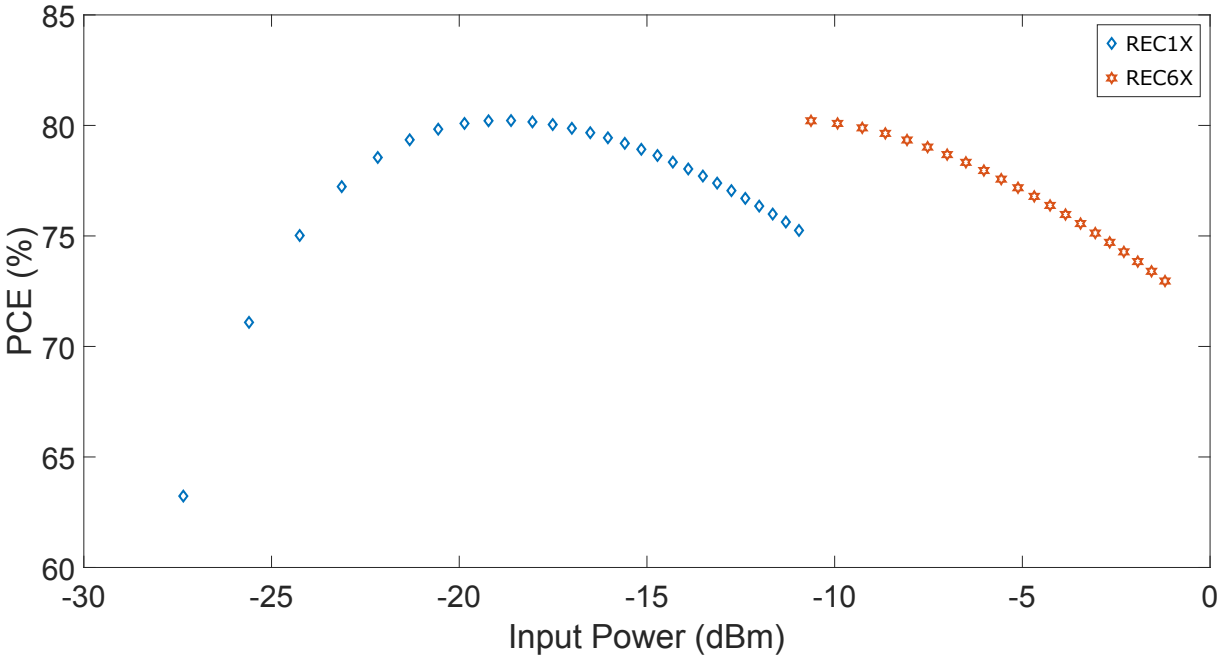


Figure 4.15. PCE of the rectifier vs. input power into the rectifier. the blue trace depicts REC1X while the red trace depicts REC6X

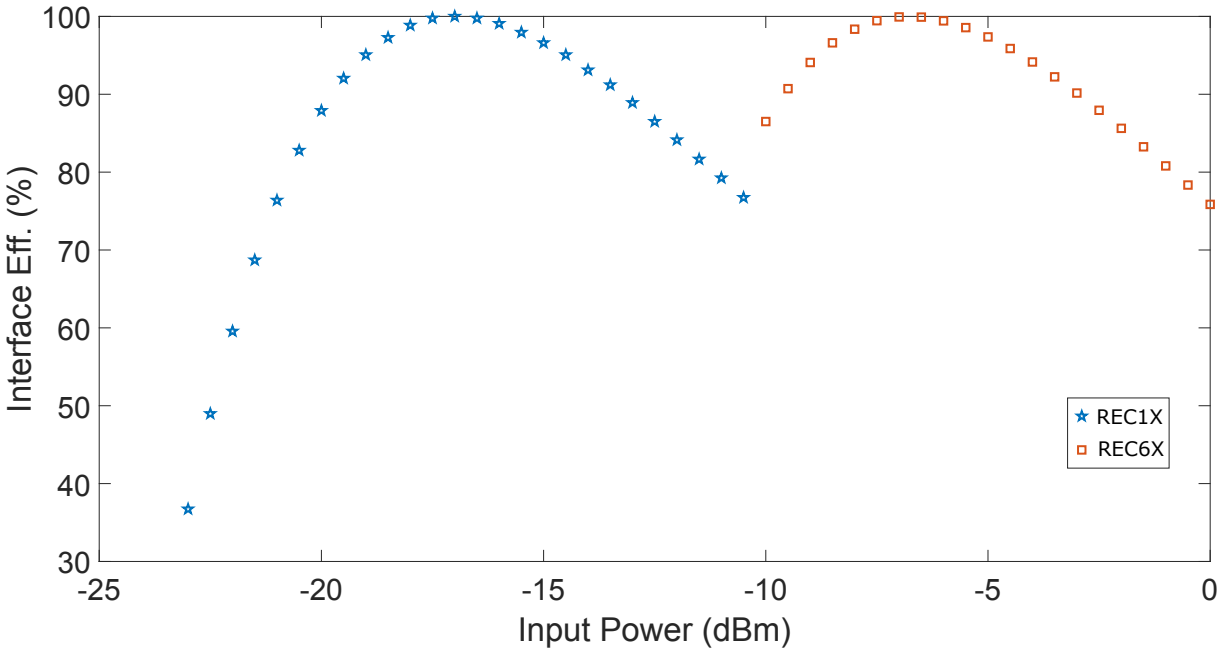


Figure 4.16. Interface efficiency vs. available input power. the blue trace depicts REC1X while the red trace depicts REC6X

Table 4.2. Performance Comparison

Design	Input Power Sensitivity	Peak Efficiency	Wideband Efficiency	Process
This Work	-23 dBm @3V Cap	80% @ -16 dBm	$>$ 60% over 20 dB	130 nm
Scorcioni et al. (2012)	-17 dBm @2V Cap	60% @ -3 dBm	$>$ 40% over 14 dB	130 nm
Stoopman et al. (2014)	-27 dBm @1V Cap	40% @ -17 dBm	N/A	90 nm
Hameed et al. (2015)	-20.5 dBm @1V 1 MΩ	20% @ -15 dBm	$>$ 20% over 7.16 dB	130 nm
Almansouri et al. (2018)	-18.3 dBm @1V 100 kΩ	66% @ -19.2 dBm	$>$ 60% over 3.5 dB	180 nm
Kotani et al. (2009)	-19 dBm @0.15V 10 kΩ	66% @ -13 dBm	$>$ 60% over 6.5 dB	180 nm

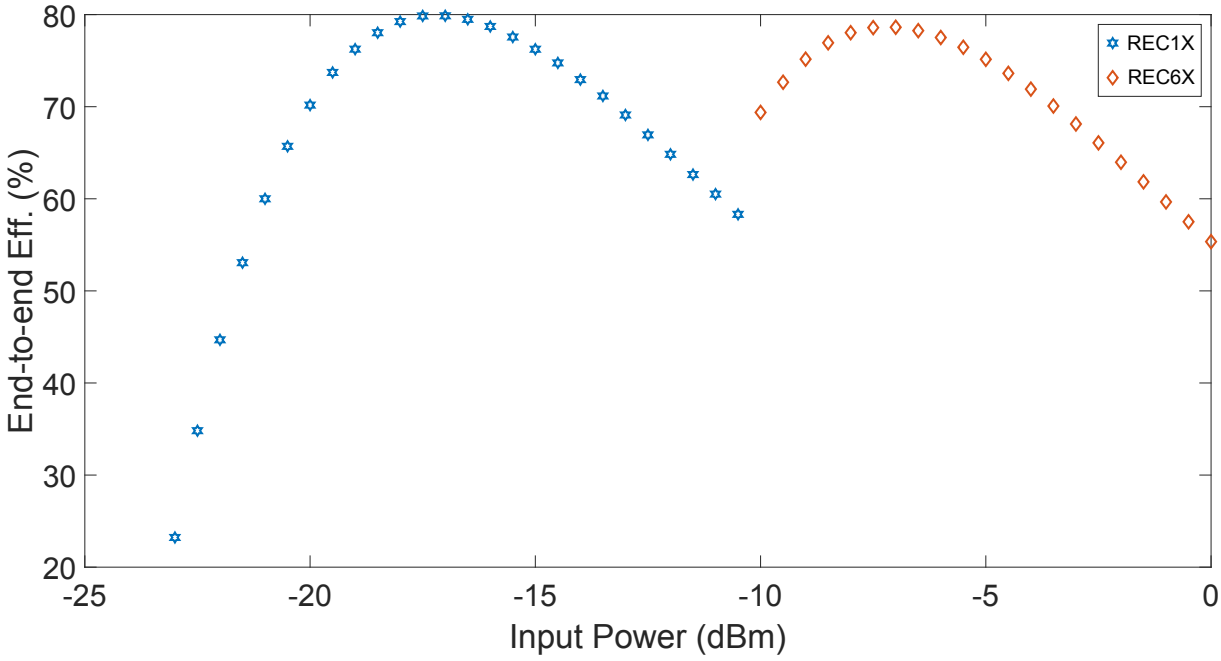


Figure 4.17. End-to-end efficiency of the complete harvester vs. available input power. the blue trace depicts REC1X while the red trace depicts REC6X

4.6 Conclusion and Discussion

In this chapter, we have proposed a novel UHF energy harvester with peak PCE tracking over a wide input power range. Our proposed design tracks the maximum PCE of threshold-compensated rectifiers through intelligently managing its output current and reconfiguration of the rectifier. The proposed harvester is implemented with the differential-drive cross-coupled rectifier, but the technique can be generalized to extend bandwidth of high conversion efficiency of many other rectifier circuits. Key contribution of this work is summarized as below:

- Fundamental studies on threshold-compensated rectifiers, identified the key limitation of the narrow high conversion efficiency input power bandwidth, due to the deep involvement of output voltage in rectification process.
- Developed a reconfiguration switching scheme that addresses the limitation and extends input power bandwidth of high conversion efficiency
- Developed an extremely efficient enable/disable mode for the UHF rectifier and relevant start-up scheme, which together made the above switching scheme possible in low input power range.

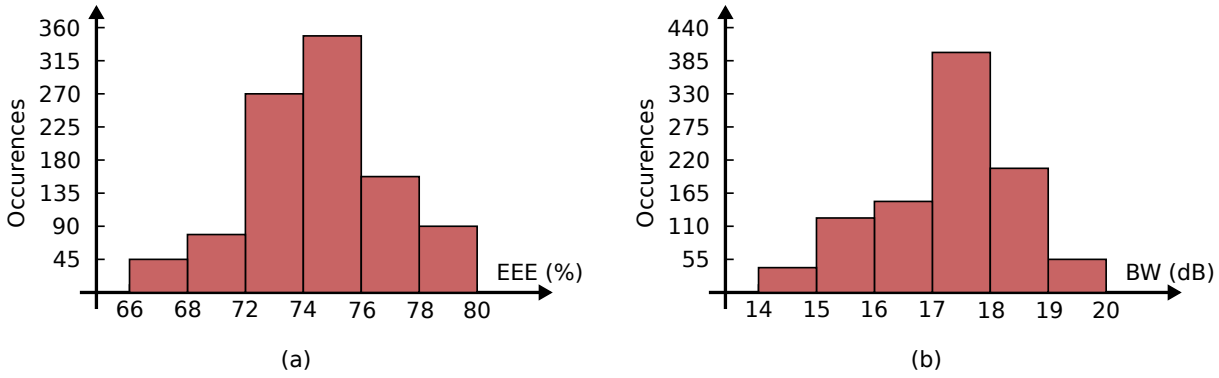


Figure 4.18. Histogram that summarizes results in joint global and local MC simulation. (a) Peak End-to-end efficiency (EEE) (b) the input power range (or bandwidth, BW) over which the EEE is more than 60%

- The resultant system eliminates dynamic reverse leakage without introducing sensitivity overhead.

In this chapter, we have identified and exploited an issue with the threshold compensated rectifier in the steady-state condition. However, the same issue is also present in the start-up transient of rectifiers and they can be exploited to improve the settling speed. This is covered in the next chapter.

Chapter 5

A Fully Integrable RF Energy Harvester with Dynamic Efficiency Tuning

IN the literature, the cold start-up speed and dynamic charging behaviour of ultra-low-power threshold-compensated rectifiers is not often addressed and is, in fact, largely ignored. In this chapter, we propose a fully-integrated UHF energy harvester realized in a 130 nm CMOS process to shorten start-up time and enhance charging speed. The proposed design relies on active sensing of the output voltage of the rectifier and dynamic reconfiguration of the rectifier. The simulation results show that the harvester is capable of charging a 1 nF capacitor to 1 V from -28 dBm input power, within 0.7 ms.

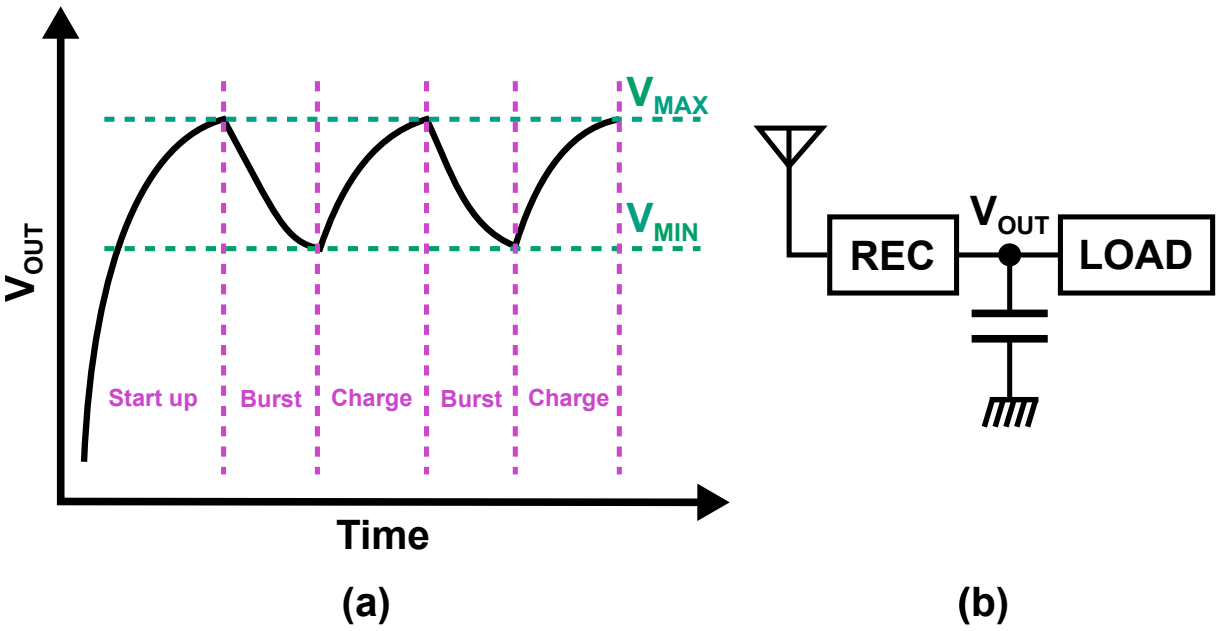


Figure 5.1. (a) Regions of operation in a charge burst system (b) A block diagram of a typical charge burst system.

5.1 Introduction

In the context of passive wireless sensor nodes, energy harvested in the UHF band is becoming increasingly common to accommodate a longer range between the base station and a wireless sensor node. In these sensor nodes, the harvested energy is accumulated via the temporary charge storage during the charge phase, and utilized by the node to perform the needed operations (e.g. sampling the analog output of a sensor, performing radio uplink and etc.) during a substantially shorter burst phase. This is often referred to as the charge-burst mode of operation and it is illustrated in Figure 5.1.

In such a system, the sensitivity of the harvester plays a vital role in the responsiveness of the system. The conventional definition of sensitivity for the power harvester is the minimum input power required to develop a certain output voltage (typically 1 V (Hameed et al., 2015)). While this definition is useful in outlining the minimum required input power for a given charge burst system to be functional, it fails to reveal the time taken to reach the final settled output voltage. As such, prior-art designs reported in the existing literature typically focuses on achieving higher input power sensitivity and tend to neglect the need for fast start-up. In (Stoopman et al., 2014), banks of weighted capacitors are added across the RF input and they are being

reconfigured during output settling to improve the input power sensitivity. At -24 dBm input power, the design is able to develop a final DC output voltage of 1.5 V but it takes more than 20 seconds for the output to settle to this final voltage. The dynamic charging behaviour is of particular concern for systems where,

- The requirement for short cold-start-up times is present.
- The output voltage of the harvester varies significantly during charge and burst cycles, in other words, a large $(V_{\max} - V_{\min})/V_{\max} \times 100\%$.

In this chapter, a novel technique for dynamic efficiency tuning is proposed and implemented as part of an UHF band harvester to significantly improve charging speed (Sun et al., 2017). We start by describing the limitation of stand-alone rectifiers in terms of dynamic charging behaviour in Section 5.2. The proposed design and simulation results are presented in Sections 5.3 and 5.4, respectively. Finally, conclusions are drawn in Section 5.5.

5.2 Limitation of stand-alone rectifiers in terms of charging behaviour

In the last chapter, we demonstrated that the power conversion efficiency of the threshold compensated rectifiers exhibits strong dependency upon its DC output voltage in the steady-state state. However, the same limitation is also present during the dynamic settling and can be potentially exploited. To elaborate on this point, two single stage rectifiers are configured either in parallel (2Xpar) or in series (2Xser), as shown in Figure 2 (a) and (b) respectively and they are simulated in the time domain to demonstrate the effect of these configurations on the input impedance and the intrinsic PCE of the rectifier during the output settling.

All the simulation data are collected in the time domain waveform, and each of the real part input impedance and the PCE of the rectifier is plotted against the output DC voltage of rectifier in Figure 5.3 (a) and (b), respectively. Observing the behaviour of the 2Xpar rectifier in Figure 5.3(b), when the output voltage of 2Xser is low, its PCE is tiny, resulting in a poor conversion efficiency at low output voltage. As V_{OUT} develops, the threshold compensation becomes effective and its conversion efficiency

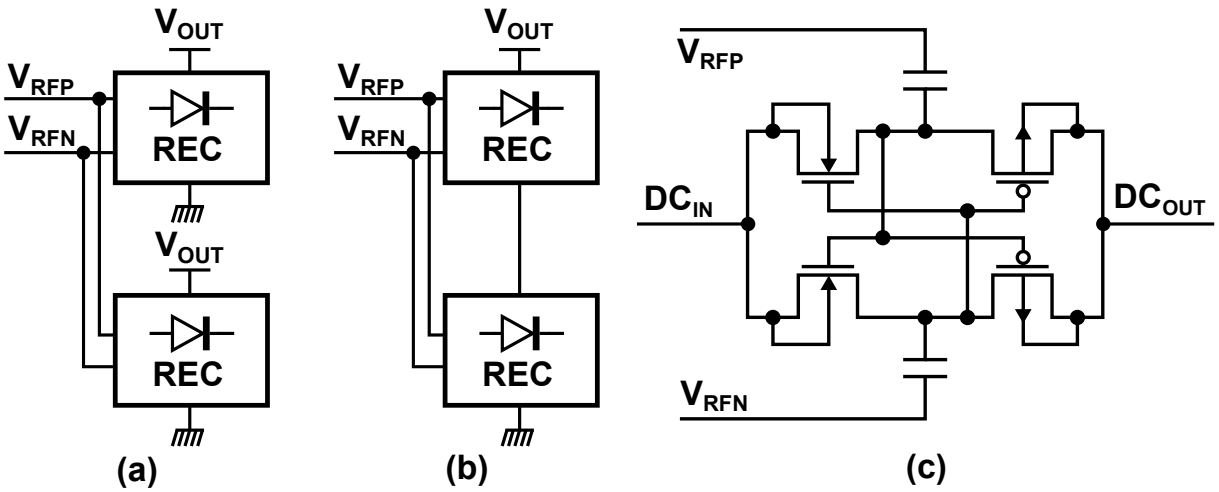


Figure 5.2. Rectifier configurations. (a) Two single rectifier stages connected in parallel (2Xpar) (b) Two single rectifier stages connected in series (2Xser) (c) The cross-coupled differential rectifier (Kotani et al., 2009) used in the simulation.

improves. Eventually, the output voltage becomes so high that the reverse leakage starts to dominate over forward conduction, resulting in a significant reduction in conversion efficiency. Similar behaviour can be observed for 2Xser as well, however, the maximum PCE occurred at an output voltage almost twice as high, because the effective voltage across the single stage rectifier of 2Xser is half of that of 2Xpar.

It is clear from the previous discussion and Figure 5.1 (b) that if the rectifier can start with 2-stage in parallel and be reconfigured into 2-stage in series around 0.46 V of the output voltage, the rectifier effectively maintains high PCE for a bigger portion of the settling process, resulting in a significantly faster charging time before the reconfiguration.

From the standpoint of the interface efficiency, in Figure 5.3(a), as the output voltage develops, the current drawn by the rectifier decreases, thus the real part of the input impedance reduces. If the rectifier is reconfigured from 2 stages in parallel into 2 stages in series at 0.46 V of output voltage, the real part input impedance is increased drastically, compensating for the falling in the real part of the input impedance. Note that the imaginary part of the input impedance is mostly due to the number of rectifier stages loaded across the RF input, thus it remains roughly unchanged irrespective of the rectifier configuration. Thus, the reconfiguration is also beneficial in the interest of maintaining a relatively constant input impedance, resulting in a better matched RF interface over the entire settling period. From the standpoint of both PCE and

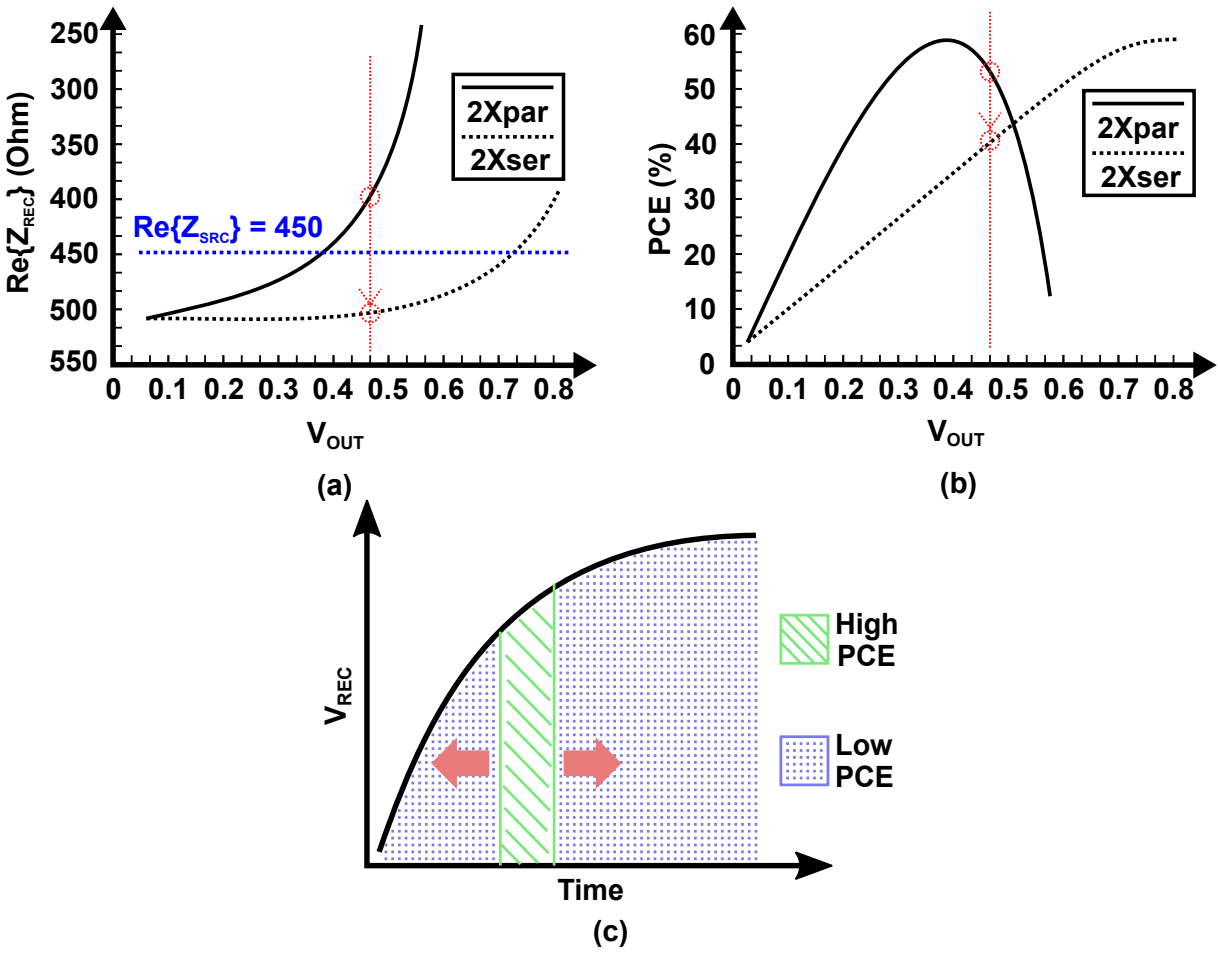


Figure 5.3. Simulation results that demonstrates the limitation of the stand-alone in dynamic settling. (a) The real part of the rectifier's input impedance vs the output voltage of the rectifier (b) the PCE vs the output of the rectifier (c) a pictorial representation of the widening high conversion efficiency zone.

the RF interface efficiency, the fore-mentioned reconfiguration scheme is beneficial for the rectifier to achieve high overall conversion efficiency for a much larger proportion of the output settling, as depicted in Figure 5.3 (c), ultimately resulting in a faster changing time.

5.3 Proposed Design

It is evident from the previous discussion that if the rectifier can be reconfigured based on its output voltage, optimal conversion efficiency can be achieved irrespective of the output voltage and the overall dynamic charging behaviour can be significantly

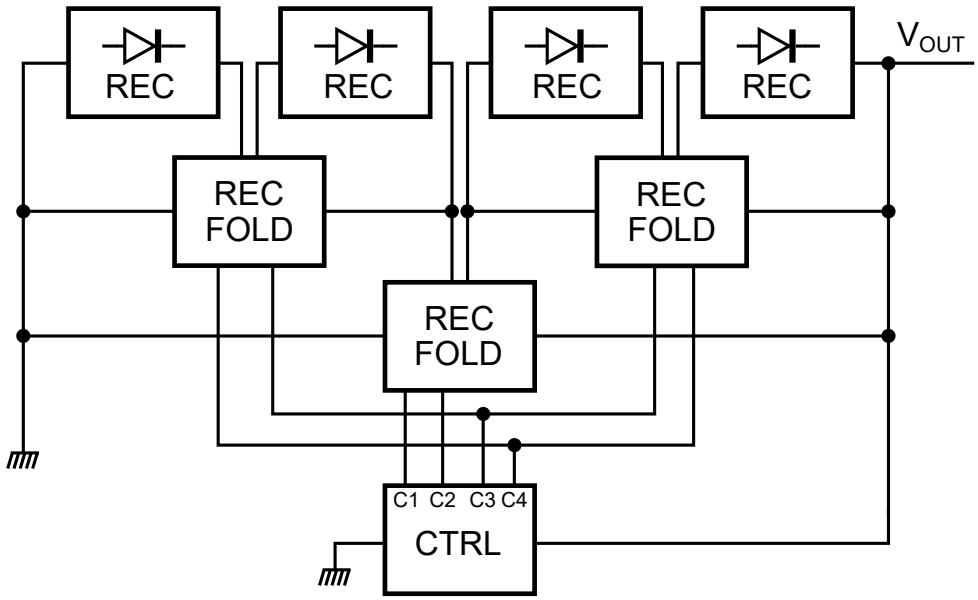


Figure 5.4. Top level schematic for the proposed design and the folding circuit that reconfigures two rectifiers to be either in series or in parallel.

improved. Based on this understanding, in Figure 5.4, the top-level schematic of the proposed design is presented. Based on the control signals, the three rectifier folding circuits, depicted in Figure 5.4, reconfigure the rectifiers into four 1-stage rectifiers in parallel, two 2-stage rectifiers in parallel or one 4-stage rectifier. The controller (CTRL in Figure 5.4) generates signals for the rectifier folding circuits by sensing V_{OUT} of the whole rectifier. The next two subsections discuss the design of the controller and rectifier folding circuit (REC FOLD).

5.3.1 Switching Decision Making Circuit

The control unit (CTRL) in the harvester provides the decision making to reconfigure the harvester from four 1-stage rectifier in parallel to two 2-stage rectifiers in parallel and the reconfiguration from two 2-stage rectifiers into one 4-stage rectifier. As depicted in Figure 5.5, the entire control unit consists of two comparators, $COMP_1$ and $COMP_2$ and an auxiliary rectifier.

If ideal switching points for reconfiguration stay constant, they can essentially be determined by comparing a divided version of the output voltage with a fixed reference voltage. However, this is not the case over the entire input power range. As the input power increases, the input voltage amplitude increases as well. Consequently, the high efficiency points tend to appear at higher output voltages, as

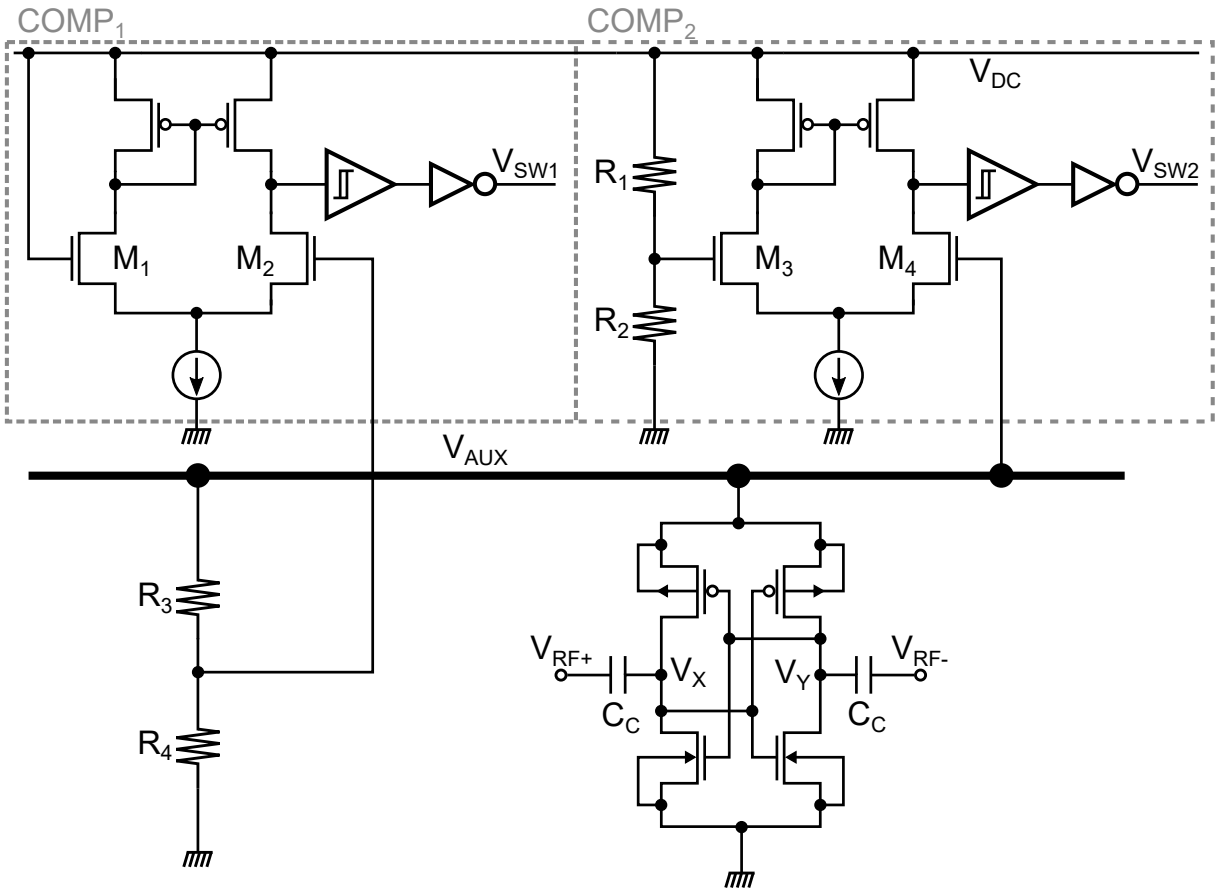


Figure 5.5. The switching decision making circuit and dynamic reference voltage generation. a single stage auxiliary rectifier is used to produce the dynamic reference voltage; the comparator used has built-in hysteresis to prevent oscillation

explained in the previous chapter. In effect, the optimal switching point is a complex non-linear function of the input RF amplitude, the threshold voltage of the transistors used in the main rectifier and the rectifier circuit topology.

To that end, as depicted in Figure 5.5, the reference voltage used with the comparators, V_{AUX}, is dynamically produced by a single-stage auxiliary rectifier. This auxiliary rectifier is implemented with four single-finger transistors, whose finger width is identical to those implemented in the main rectifier. This is done so that the auxiliary rectifier best mimics the main rectifier in terms of the developed output DC voltage. This output voltage is then used with a comparator as an indicator of the reconfiguration switching point.

As shown in Figure 5.5, there are 2 voltage comparators. The comparator $COMP_1$ detects the switching point from 4 one-stage rectifiers in parallel to 2 2-stage rectifiers

in parallel while the comparator $COMP_2$ detects the switching point from 2 2-stage rectifiers in parallel to a single 4-stage rectifier. To achieve a switching threshold 85% of V_{AUX} in $COMP_1$, the supply voltage is compared against a divided version of V_{AUX}, generated by a voltage divider consisting of R_3 and R_4. In $COMP_2$, we need to achieve a switching threshold roughly 85% of $2V_{AUX}$ and this can be easily achieved by appropriately sizing the resistors R_1 and R_2 in the supply voltage divider. Through extensive simulation experiments, it has been found that the settling speed of the single-stage rectifier deteriorates significantly after the rectifier reaches the 85% of the maximum achievable output voltage. It is also noted that, as with most ultra-low-power designs, R_1, R_2, R_3 and R_4 are realized with a string of diode-connected transistors operating in the deep sub-threshold region to achieve a better trade-off between area and power consumptions.

5.3.2 Start-up Consideration and Implementation of the REC FOLDs

In the initial condition, the DC output voltage of the whole harvester system is zero. Thus, the voltage needed to turn-on/off the rectifier configuration switches are not in place. Note that this issue was resolved in previous chapter by having a start-up rectifier that develops the needed voltage to drive the reconfiguration switches. However, the priority then was the steady state performance of the system while the start-up and dynamic performance of the system is more crucial in this design. Hence, in this work, device choices in the REC FOLD are made such that the system is pre-configured as 4 1-stage rectifiers in parallel at system start-up. Specifically, in REC FOLD shown in Figure 5.6 (d) the transistor M_2 and M_3 folds the two rectifiers in parallel, hence they are implemented with native transistors to ensure that they are on initially. On the other hand, the transistor M_1 which configures the two rectifiers in series is implemented with nominal V_{TH} transistor to ensure that it remains off during the initial power-up.

After V_{OUT} reaches the switching level, the respective REC FOLD circuit needs to reconfigure the serially connected rectifier to be in parallel. Hence, we need a negative V_{GS} and V_{SG} to turn off M_2 and M_3 respectively and a positive V_{SG} to turn on M_1. These are achieved through auxiliary rectifiers and level shifters, as illustrated in Figure 5.6 (a), (b) and (c). In part (a), the output of the 3-stage rectifier is referenced to the start of the second stage (2nd-str), hence this rectifier generates a voltage lower than 2nd-str, the long NMOS pulls M_{1G} to the low voltage generated by the auxiliary rectifier when

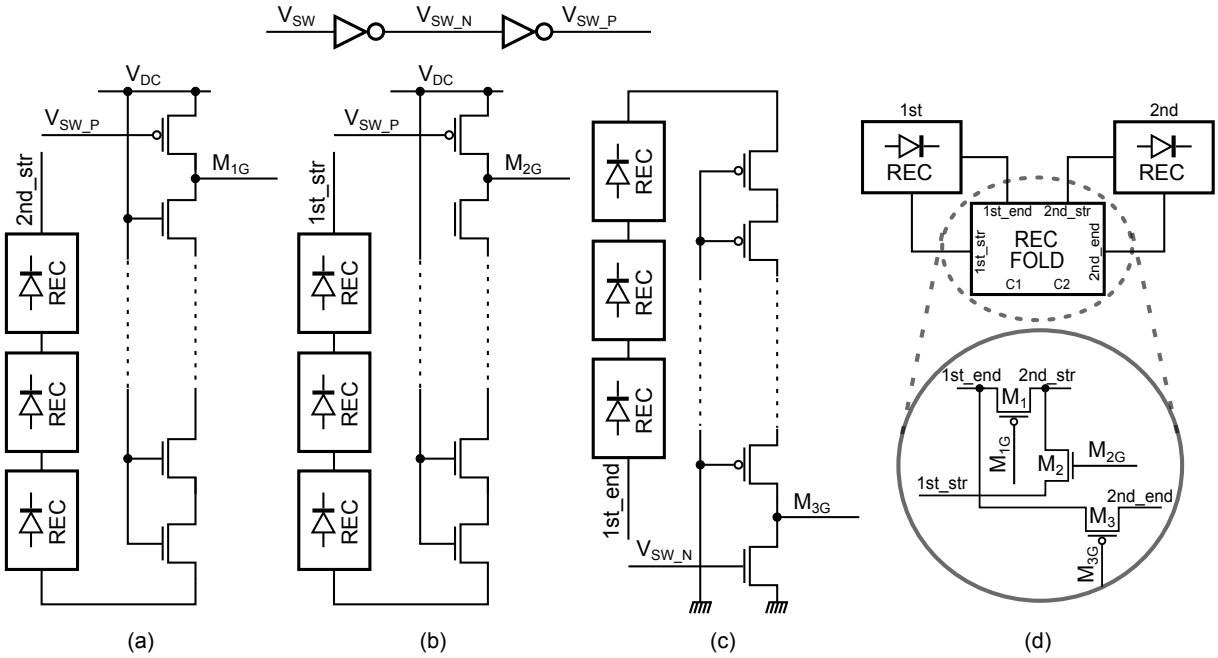


Figure 5.6. The schematic of the REC FOLD circuit.

the top PMOS is off. In part (b), the output of the 3-stage rectifier is referenced to the start of the first stage (1st-str), hence this rectifier generates a voltage lower than 1st-str. The long NMOS pulls M_{2G} to the low voltage generated by the auxiliary rectifier when the top PMOS is off. In part (c), the input of the 3-stage rectifier is referenced to the end of the first stage (1st-end), hence this rectifier generates a voltage higher than 1st-end, the long PMOS pulls M_{3G} to the high voltage generated by the auxiliary rectifier when the bottom NMOS is off.

5.4 Simulation Results

In Figure 5.7, the simulation transient of both proposed 4-stage reconfigurable rectifier and the fixed 4-stage rectifier are conducted at 915 MHz at -24 dBm input power, with a custom source impedance of $28 + j350\,\Omega$ (i.e. an antenna with this custom impedance is required). It can be seen that the proposed reconfigurable rectifier settles significantly faster than the fixed 4-stage counterpart. The 90% settling time of the proposed rectifier has been reduced by more than 50%, with respective to the fixed 4-stage rectifier.

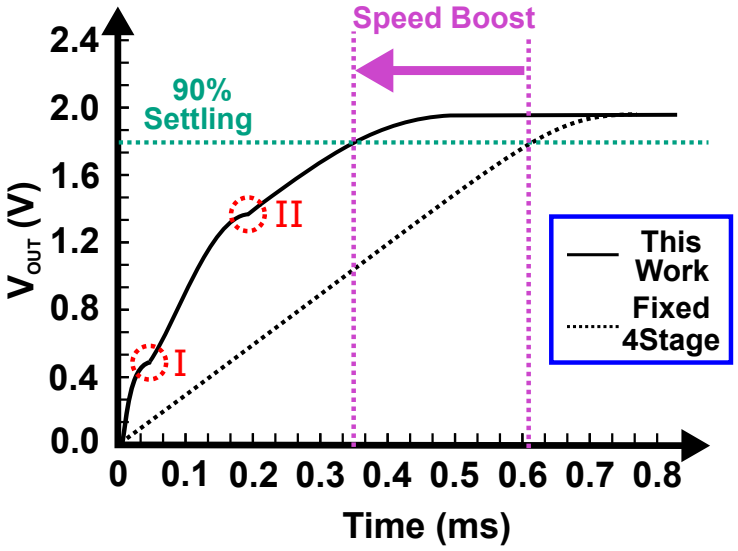


Figure 5.7. Simulation transient of the reconfigurable 4-stage rectifier vs. a fixed 4-stage rectifier. 1 nF load capacitor is used. The configuration from 4 1-stage rectifiers into 2 2-stage rectifiers, and the reconfiguration from 2 2-stage rectifiers into 1 4-stage rectifier occur at (I) and (II), respectively, as annotated by the red circles

In addition, we have simulated the charging time of the proposed reconfigurable 4-stage (using adaptively generated V_{REF}) vs the fixed 4-stage design and the charging time of the proposed reconfigurable 4-stage (using fixed V_{REF}) vs the fixed 4-stage design. Both simulations have been conducted from an input power of -18 dBm down to -30 dBm and the speed boost factors (i.e. proposed adaptive approach over conventional fixed approach) are recorded in Table 5.1. From Table 5.1, it can be observed that the reconfigurable 4 stage (adaptive V_{REF}) charges the output capacitor faster than the fixed 4-stage rectifier over the entire simulated input power range. Additionally, although the speed boost factor of the reconfigurable design (fixed V_{REF}) is close to that of the design with dynamically generated V_{REF}, its speed advantage quickly diminishes as we move away from -24 dBm input power where the fixed reference voltage is optimized for and eventually surpassed by the conventional fixed 4-stage design as the input power exceeds -20 dBm.

5.5 Conclusion

This chapter presents a fully-integrable UHF harvester that achieves improved dynamic charging speed through intelligent reconfiguration based on its output voltage. In Table 5.2, it can be seen that the proposed reconfigurable harvester

Table 5.1. Performance Comparison (Adaptive V_{REF} vs Fixed V_{REF})

P_{IN} (dBm)	Speed Boost Factor (Adaptive V_{REF})	Speed Boost Factor (Fixed V_{REF})
-18	1.55	0.54
-20	1.60	1.03
-22	1.66	1.38
-24	1.74	1.75
-26	1.68	1.41
-28	1.57	1.12
-30	1.51	0.64

Table 5.2. Performance Comparison (with prior-art designs)

Design	Input Power Sensitivity	T_{charge}	Technology
This Work	-28 dBm @1 V	0.7 ms (1 nF)	130 nm CMOS
(Oh et al., 2012)	-27 dBm @1 V	1.7 ms (1 nF)	130 nm CMOS
(Stoopman et al., 2014)	-24 dBm @1.6 V	23 s (N/A)	90 nm CMOS

achieves superior charging speed, without significantly compromising the input power sensitivity, compared with prior-art designs.

The contribution of this work are as follows:

- We proposed a rectifier that reconfigures itself based on the output voltage to speed up its settling process. The configuration is done given the knowledge of the tight trade-off between forward passing and reverse leakage.
- The proposed dynamic reference voltage generated by the auxiliary rectifier provided a more accurate representation of the optimized switching threshold in a realistic application scenario, resulting in a robust design.
- Innovative rectifier folding circuit is proposed to realize the dynamic reconfiguration and multi-V_{TH} technology has been exploited to resolve the difficulty of turn-on at start-up.

In the next chapter, we discuss the issues with the power management in an energy harvesting system. In particular, we focus on managing the instances when the harvested power is insufficient as well as the instances when the harvested power in excess, and discuss how this can be exploited to improve the system performance.

Chapter 6

A Fully Integrated HPMU for Passive UHF RFID

THIS chapter presents a fully integrated hybrid power management unit (HPMU) realized in the 130 nm CMOS. The design improves the performance of RFID tags—especially those with passively powered sensors—by intelligently managing harvested power. The HPMU opportunistically takes advantage of the excess harvested power beyond the operational requirements of a tag and stores this energy externally. Through smart power routing, this stored energy is used to sustain the supply voltage of tag circuitry. This approach can reduce cold start-up time, mitigate consequences of brownouts and, effectively, extend the operational range and the responsiveness of tags—especially those with passively powered sensors. In addition, the HPMU switches off when the harvested power, indicative of a weak interrogating signal, is too low to conserve stored power. The entire HPMU has been optimized for low power consumption, which not only reduces the power overhead that HPMU introduces, but also ensures that as much power as possible is siphoned and stored rather than dissipated in the power management circuitry. In the OFF state, the HPMU consumes only around 10 nA from the external storage element.

6.1 Introduction

Traditionally, in the context of a fully passive (batteryless) RFID tag, the excess power above that required for tag circuity operation is not utilized. As the input power increases—for instance when the distance between an RFID tag and an interrogating antenna is reducing—the rectified DC output voltage increases. The role of a linear regulator at the rectified output is to ensure a consistent supply voltage level for tag digital logic circuitry and the tag does not benefit from occurrences of higher rectified DC output. The ability to exploit such excess harvested energy is especially significant where sensors are increasingly interfaced with passive RFID technology to realize the benefits of batteryless sensing in a wide range of applications from healthcare to structural health monitoring (Yeager et al., 2009; Torres et al., 2013; Beriain et al., 2014; Jauregi et al., 2017; Wickramasinghe et al., 2017).

Another problem facing applications built on purely passive RFID tags is unintentional brownouts where the power level at the output of the rectifier can drop significantly within a short period of time due to, for example, unpredictable field nulls and possible misalignment between the tag's antenna and the reader's antenna (Dong et al., 2015). In addition, cold start-up—time to respond to an interrogation signal by a powered down RFID tag—is typically longer with fully passive tags and consequently reduce the overall responsiveness of tags, especially those tags with integrated sensors (Sample et al., 2008; Ussmueller et al., 2012; Su et al., 2015; Sample et al., 2011).

In (Dong et al., 2015), a new concept was proposed to take advantage of excess harvested power and address the problem of brownout whilst also reducing the cold start-up time of a sensor enabled passive RFID tag. The operational principle is illustrated in Figure 6.1. Specifically, when the tag is close to an interrogating antenna, harvested power is used to power the tag circuitry and charge an external energy storage device such as a super capacitor, *ie* passive and charging mode of operation. When the harvested power drops below the operating conditions of the tag circuitry, external storage is routed to power the tag, *ie* semi-passive mode of operation. If the RF (radio frequency) field strength detected at the tag is too low and suggestive of a backscattered response not being successfully received and decoded by an RFID reader, the tag is turned off to preserve the energy in the external energy storage device, *ie* off mode.

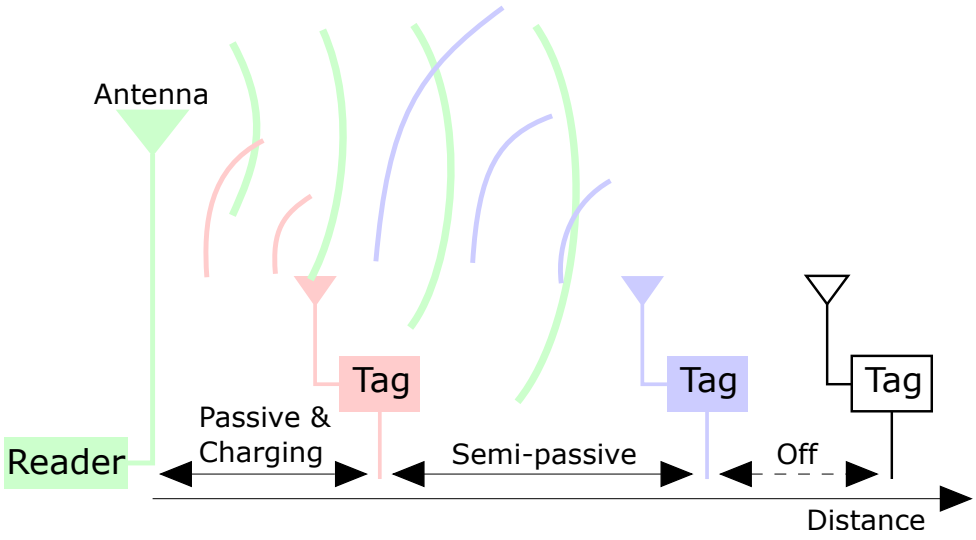


Figure 6.1. Modes of operation of the hybrid power management concept.

In this chapter, we design a new power management that realizes the above mentioned concept (Sun et al., 2017,0), the contribution of this work is summarized as follows,

- A fully integrated hybrid power management unit (HPMU) is designed to intelligently utilize harvested power. The HPMU strategically routes excess harvested power to an external power storage element while maintaining adequate power to execute tag functions, and routes this stored energy back to power the tag when the harvested power is insufficient. When the incident RF field sensed by the HPMU is determined to be inadequate to successfully backscatter a tag response, power from the external storage is switched off.
- The fully integrated hybrid power management unit is realized using a GlobalFoundaries 130 nm process and simulation-based experiments are conducted in Cadence Virtuoso Simulation Environment to demonstrate the functional behaviour of the HPMU and evaluate the power consumption of the power management unit as well as its power conversion efficiency (PCE). It is shown that an optimal PCE of approximately 65% can be achieved with only a negligible power overhead due to the HPMU.

The remaining sections of the chapter are organized as follows: Section 6.2 describes the overall design of the HPMU; Section 6.3 and Section 6.4 discuss the design of the two critical functional blocks within the HPMU: the excess energy management unit (EEMU); and the power routing unit (PRU), respectively. Section 6.5 presents the

simulation based experimental results of the proposed design; Section 6.6 discusses related work and Section 6.7 concludes the chapter.

6.2 HPMU Design Overview

A high-level illustration of the proposed HPMU, including the central functional blocks, is depicted in Figure 6.2. First, the rectifier converters the RF input energy into a DC output voltage, V_{REC}. A current feeder (CF) controls the amount of current the current controlled oscillator (CCO) and the charge pump pulls from V_{REC} to regulate V_{REC} at a voltage desired by the LDO (low dropout) linear regulator. The current-controlled oscillator drives the charge pump to deliver charge to the external energy storage element. On the other hand, the power routing unit (PRU) routes either the rectified power or the stored power in the energy storage element to the LDO to power the load—in the illustration a microcontroller (MCU) such as that used in the Wireless Identification and Sensing Platform (WISP) (Sample et al., 2008). In addition, the voltage reference generator produces a constant V_{REF} for the rest of the system where a supply independent reference voltage is needed.

The power routing decisions depends on V_{REC} as well as the output of the energy storage element, V_{STOR}. Specifically, when V_{REC} is 2.5 V or above the rectified power is routed to power the LDO, when the V_{REC} is below 2.5 V and V_{STOR} indicates the storage is not empty, the stored power is routed to power the LDO to prevent a sudden power loss or brownout event. The 2.5 V threshold was chosen to provide enough voltage headroom for the operation of a typical off-the-shelf LDO and MCU. When V_{REC} falls below 1 V, the system switches off as such a low voltage indicates that the tag is sufficiently far away from an interrogating antenna to successfully receive a tag response. When V_{REC} rises above 1 V, the system can be booted from the stored power to significantly reduce the cold start-up time.

The following sections present, in detail, the two major functional blocks: i) the excess energy management unit (EEMU); and ii) the power routing unit (PRU) of the HPMU.

6.3 Excess Energy Management Unit

The block-level diagram of this functional block is depicted in Figure 6.3. The output of the amplifier AMP_1 is connected to the gate the transistor P_1 and P_2. P_1 provides

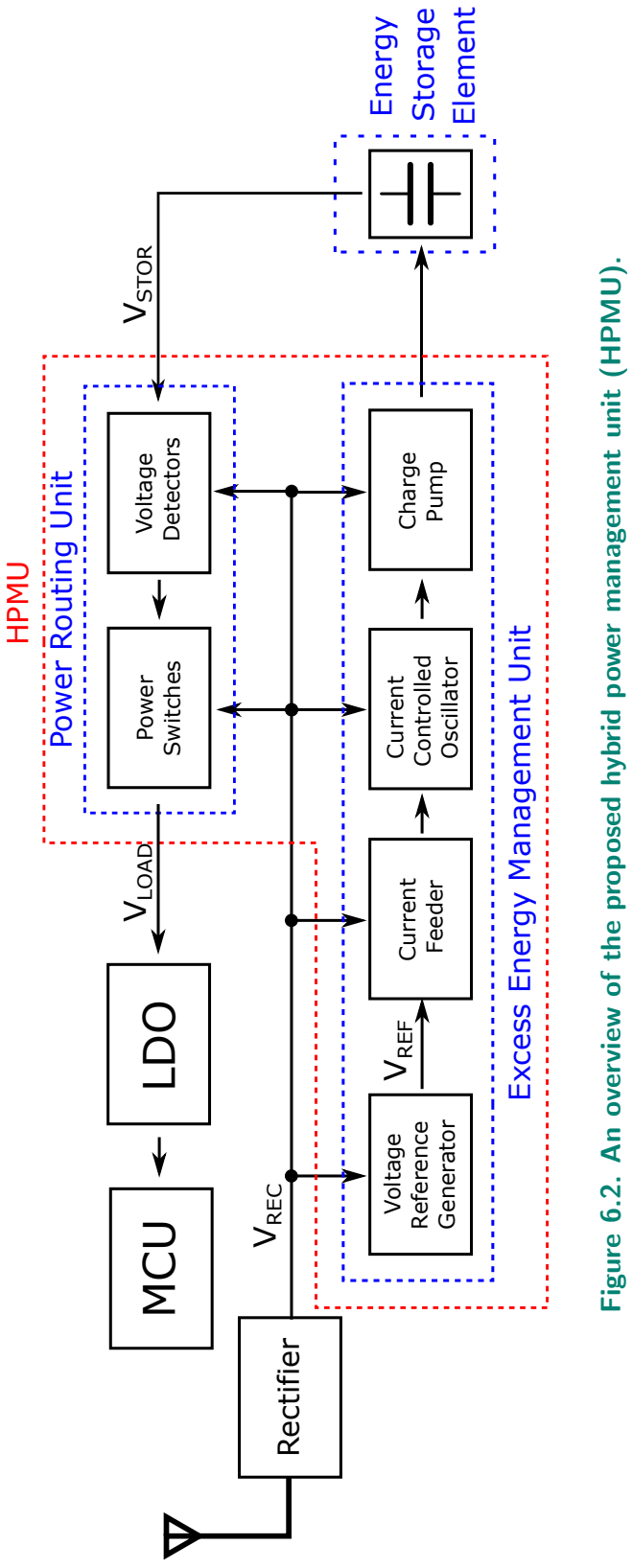


Figure 6.2. An overview of the proposed hybrid power management unit (HPMU).

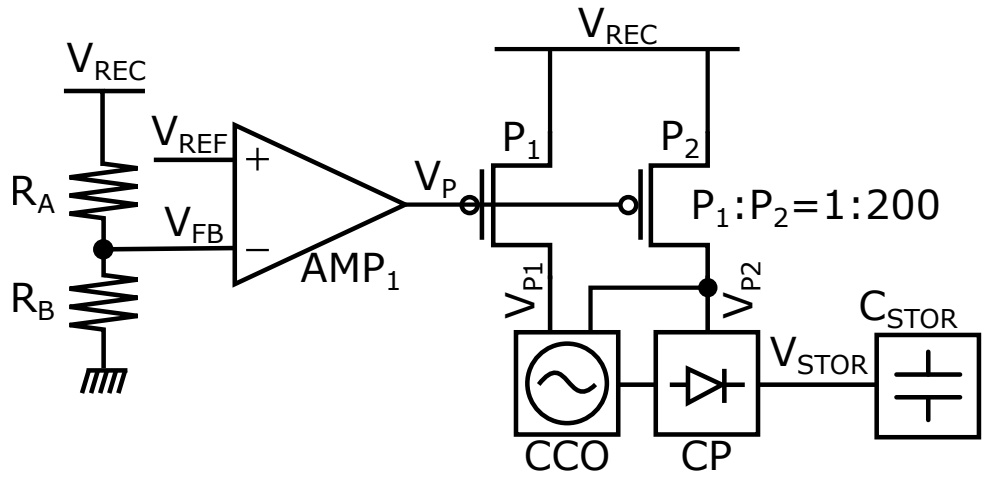


Figure 6.3. The excess energy storage unit together with a super capacitor C_{STOR} as an energy storage element.

the control current for the CCO while P2 provides the needed current for the rest of the CCO and the charge pump (CP). A divided version of the V_{REC}, V_{FB} is connected to the negative input of the amplifier AMP_1, forming a negative feedback loop, which regulates V_{REC} to be 2.5 V. When input power increases, the excess power increases and V_{REC} tends to rise, subsequently V_{FB} becomes larger than V_{REF} and the output of the amplifier AMP_1 decreases. This results in more current drawn from V_{REC}, preventing V_{REC} from increasing. On the other hand, when input power decreases, V_{REC} tends to drop, V_{FB} falls below V_{REF}, AMP_1 increases V_P to reduce the current pulled from V_{REC}, resisting V_{REC} from reducing. The amount of current available to the CCO determines its oscillation frequency, which in turns determines the energy stored in the external storage element per unit time. Effectively, the more excess power there is, the more power will be pumped into the external storage element. In order to reduce power consumption and save chip area, a voltage divider (*ie* R_A and R_B in Figure 6.3) is realized using a string of diode-connected PMOS transistors.

As the input RF power varies, V_{REC} could potentially increase up to 4 V. Thus, excellent line regulation is required to ensure the correct operation of EEMU. In (Seok et al., 2012), a 2-T voltage reference generator is proposed to provide a reference voltage based on the difference between the threshold voltages of a high V_{TH} NMOS and a low V_{TH} NMOS, as shown in Figure 6.4(a). Inspired by (Seok et al., 2012), in this work, we designed a PMOS equivalent 2-T voltage reference generator—Figure 6.4(b)—and a cascode voltage reference—Figure 6.4(c)—based on both the NMOS 2-T and the re-designed PMOS 2-T references, achieving outstanding line regulation and higher

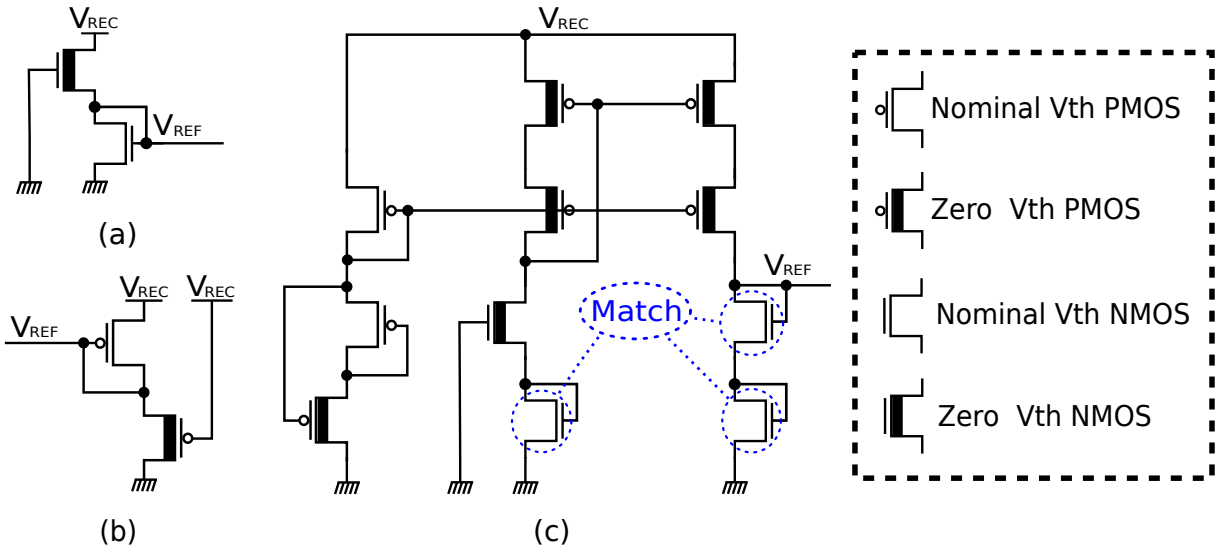


Figure 6.4. The voltage reference generator. (a) The portable 2-T voltage reference generator proposed in (Seok et al., 2012). (b) The re-designed PMOS version of the voltage reference generator (c) The cascoded voltage reference generator that employs both NMOS and PMOS version of the 2-T voltage reference generator

reference voltage level. In Figure 6.4(b), the generated V_{REF} is with respect to the V_{DD} rather than the ground. In Figure 6.4(c), the current produced by the NMOS 2-T reference is mirrored over to the right branch and is passed through two matching diode-connected NMOS transistors, thus two times the reference voltage can be achieved. The simulation transient of the cascode voltage reference is shown in Figure 6.5, and it can be observed that the output reference settles to around 0.6 V after the supply voltage exceeds 1 V.

The design of current controlled oscillator is depicted in Figure 6.6. To achieve a low power design, the CCO consists of a current starved inverter, a Schmitt trigger and an inverter to provide the additional phase shift. The CCO output is fed to two inverters which provide enough current capability to drive the charge pump, as shown in Figure 6.7.

The charge pump, shown in Figure 6.7, employs a cross-coupled differential-drive structure which achieves higher efficiency than the classical Dickson charge pump (Kotani et al., 2009). Due to the relatively high differential input, parasitic diodes of transistors can be easily turned on, degrading the efficiency and reliability of the circuit. Thus, as shown in Figure 6.8, two auxiliary PMOS transistors are used to bias the bulk of every PMOS transistor in the main rectification chain to the higher of the

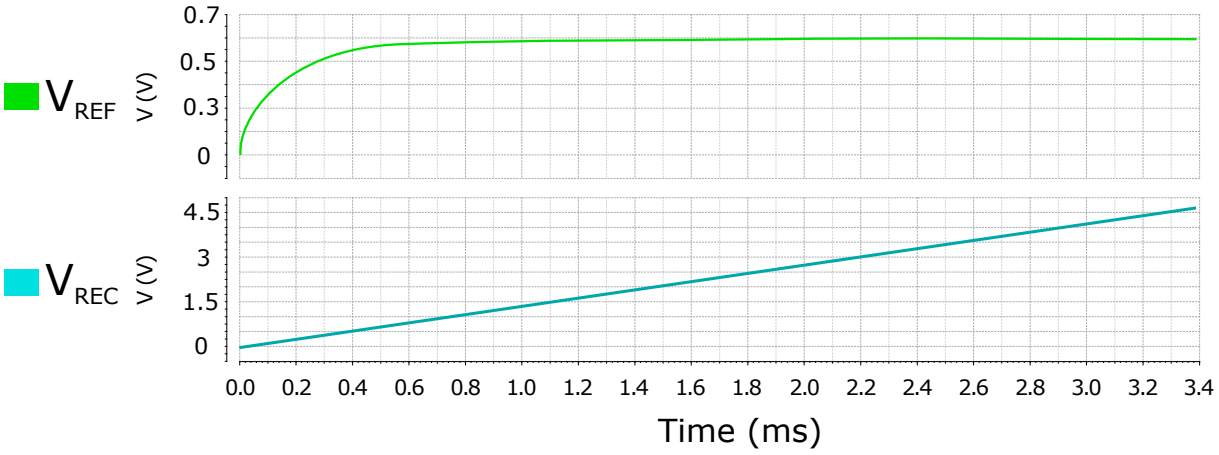


Figure 6.5. The simulation transient of the cascode voltage reference generator.

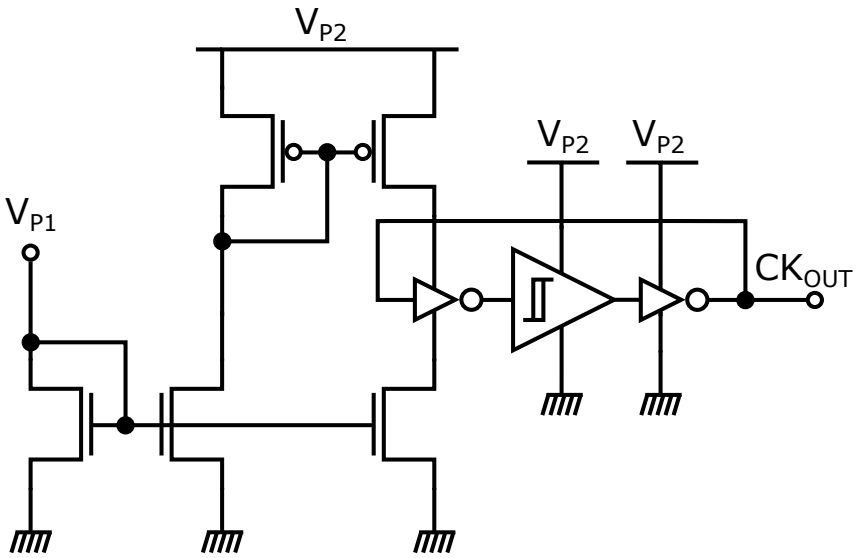


Figure 6.6. The low power current controlled oscillator (CCO).

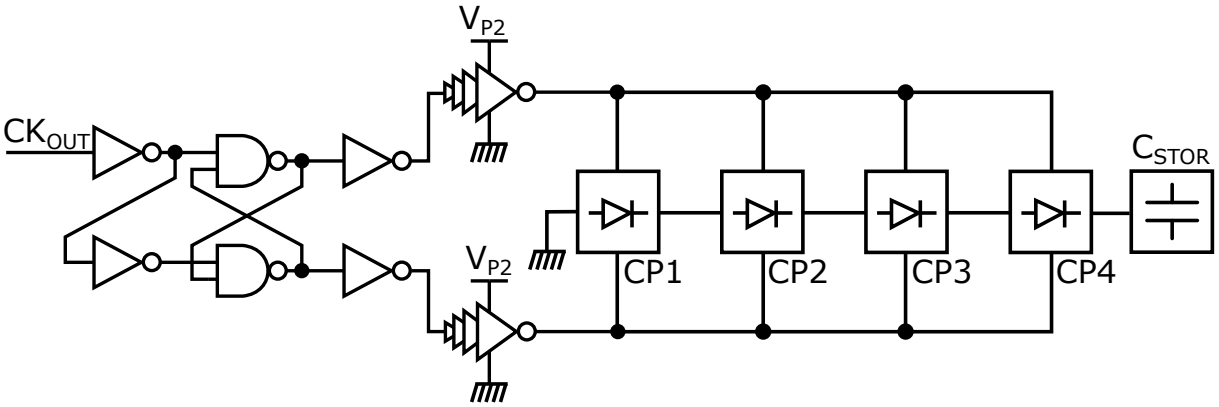


Figure 6.7. The four-stage charge pump (CP).

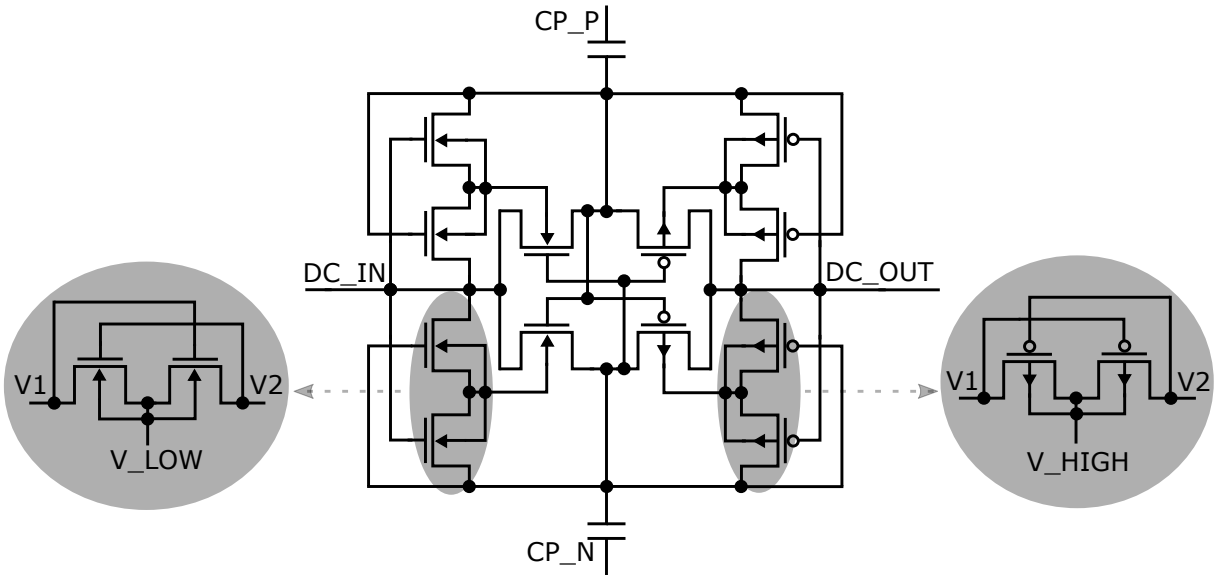


Figure 6.8. A single differential drive rectifier stage with dynamic bulk biasing used for the first three charge pump stages—CP1 to CP3—illustrated in Figure 6.7.

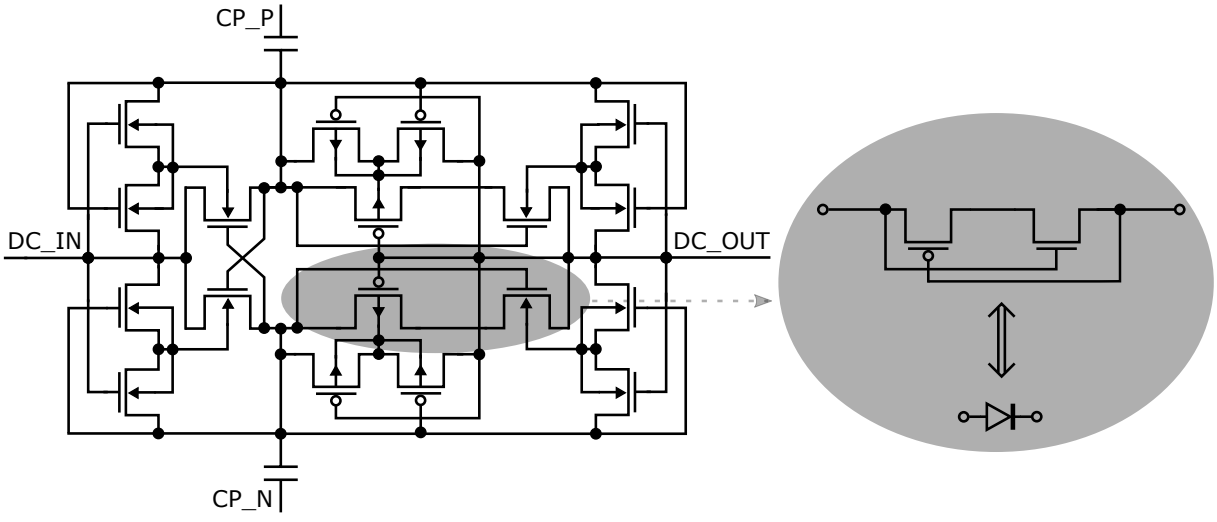
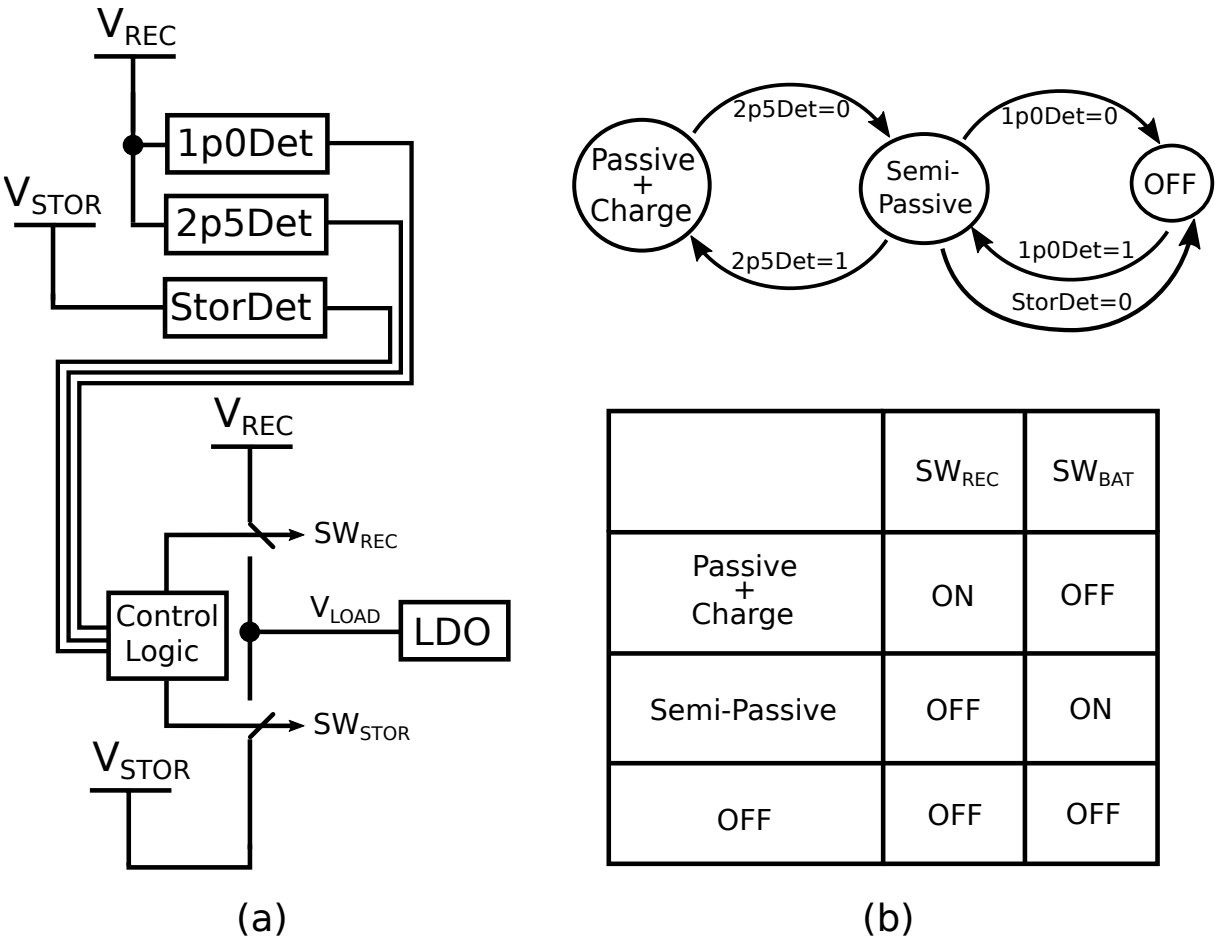


Figure 6.9. The last charge pump stage—CP4—implemented with complementary CMOS diodes to prevent reverse leakage.

input AC or the output DC. Similarly, two auxiliary NMOS transistors are used to bias the bulk of every NMOS transistor in the main rectification chain to the lower of the input AC or the input DC voltage. Using these configurations, the bulk terminal of all transistors is biased such that no parasitic diodes can be turned on. The last stage of the charge pump, as shown in Figure 6.9 exploits complementary CMOS diodes (Stoopman et al., 2014) to prevent reverse leakage and loss of charge already stored in an energy storage element. Similar to the previous stages, the PMOS and NMOS pairs are also exploited in the last stage—CP4 in Figure 6.7 and Figure 6.9—for appropriate bulk biasing. It is also worth mentioning that the voltage level of the storage element is clamped at around 4 V to avoid over-charging. The 5 V tolerant devices in the process are employed for circuits that need to operate at these high voltages.



	SW_{REC}	SW_{BAT}
Passive + Charge	ON	OFF
Semi-Passive	OFF	ON
OFF	OFF	OFF

Figure 6.10. The power routing unit (PRU). (a) The top-level block diagram of the PRU (b) Control logic of the power routing unit for the operating modes illustrated in Figure 6.1.

6.4 Power Routing Unit

As shown in Figure 6.10 (a), the power routing unit consists of a 1 V voltage detector (`1p0Det`) and a 2.5 V voltage detector (`2p5Det`) for the rectified DC output voltage and an energy storage element voltage detector (`StorDet`) which asserts output at 3.6 V and de-asserts its output at 2.5 V. The output of three voltage detectors are fed into the control logic to determine the control signals to the two switches SW_{REC} and SW_{STOR} to realize the active power routing as discussed in Section 6.1. The control sequence of the logic circuitry is depicted in Figure 6.10 (b).

Amongst the three voltage level detection circuits, both the 1 V detection and energy storage element voltage level detection are designed to operate with very little power in all modes of operation highlighted in Figure 6.10 (b). On the other hand, the 2.5 V voltage detector is designed to operate with low power in semi-passive mode and off mode. In the semi-passive and charging mode, however, more current is consumed to improve the speed of detecting the rectified output voltage falling below 2.5 V, which initiates power re-routing from external storage to mitigate brown-out. Detailed implementation of this voltage level detection circuit is shown in Figure 6.11(a). In Figure 6.11(a), when V_{REC} rises above 2.5 V, its divided version V_{DIV} exceeds V_{REF}, V_{DETN} is pulled to ground and the PMOS switch P_3 is closed, thus additional bias current is provided to PMOS differential pair (P_1 and P_2) to improve speed. In contrast, when the rectifier output voltage falls below 2.5 V, the additional bias current into the differential pair is removed, reducing the standby power consumption. In addition, the voltage divider as shown in Figure 6.11(b), realized with 15 diode-connected PMOS transistors operating in deep sub-threshold region, can be reconfigured, based on V_{DETN} to provide hysteresis for the voltage detector shown in Figure 6.11(a).

The design of the power routing circuitry requires solving three key challenges: i) the design of control logic circuits requiring voltage translation to translate logic levels based on two different and varying supply voltages; ii) the design of power switches; and iii) the design of digital logic circuits with low peak current.

A resistively loaded common source stage shown in Figure 6.12 is used as the voltage level translation structure. When V_{IN} is low, the resistor at the drain of the transistor pulls the node V_{OUTN} to be the supply voltage to be translated to, then the inverter pulls V_{OUT} to ground. On the other hand, when V_{IN} is high, the NMOS transistor N_1 is turned on to pull the node V_{OUTN} to ground, then the inverter pulls V_{OUT} to the supply voltage to be translated to, *ie* V_{TRAN}. This structure allows us a translation

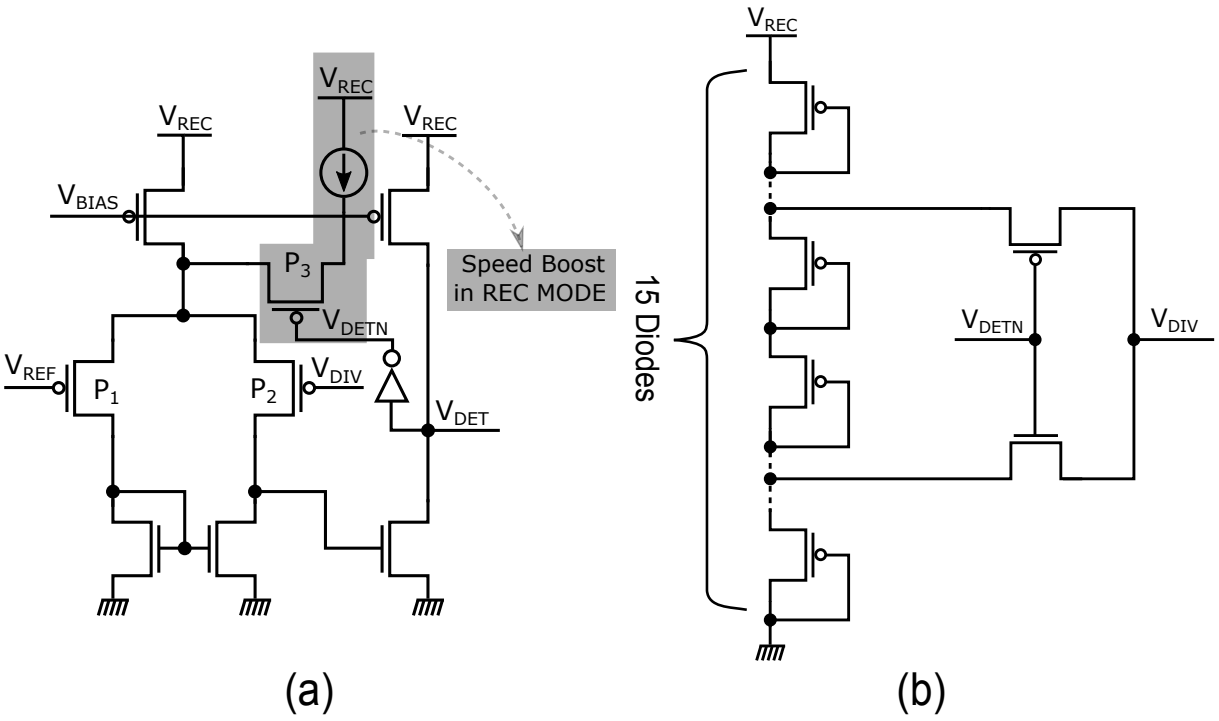


Figure 6.11. The voltage detector. (a) 2.5 V threshold detection circuit with a response speed boost in Passive and Charging mode (b) a reconfigurable voltage divider that provides hysteresis

between the two supplies (i.e. V_{REC} and V_{STOR}) that are not only different but also varying. The voltage translation is needed to ensure the proper operation of the control logic under all conditions. Conventionally, the load resistor in Figure 6.12(a) is realized using stacked PMOS transistors with the gate terminal of each PMOS transistor tied to ground, as shown in Figure 6.12(b). However, thick oxide devices are used to cope with high supply voltages (3 to 4 V) and their minimum width is limited to 0.5 um, resulting in a very long device if ultra-low-current through the resistor is desired. As such, the topology shown in Figure 6.12(c) is used to achieve reduced current with small area. In Figure 6.12(c), the gate terminal of the three transistors in the stack is no longer pulled to ground. Instead, they are biased through a voltage divider, realized using a string of diode connected transistors. This results in a significant reduction in the over-drive voltage of the PMOS transistors, subsequently, a drop in the needed length to achieve the same low current consumption as the conventional approach with very long devices.

The proposed design for the power switch is shown in Figure 6.13 (a). It is designed to ensure when the gate of the PMOS switch P_{SW} is pulled high, the control signal V_{CONT} of the PMOS switch comes from the higher of the two supply voltages, which are V_{REC}

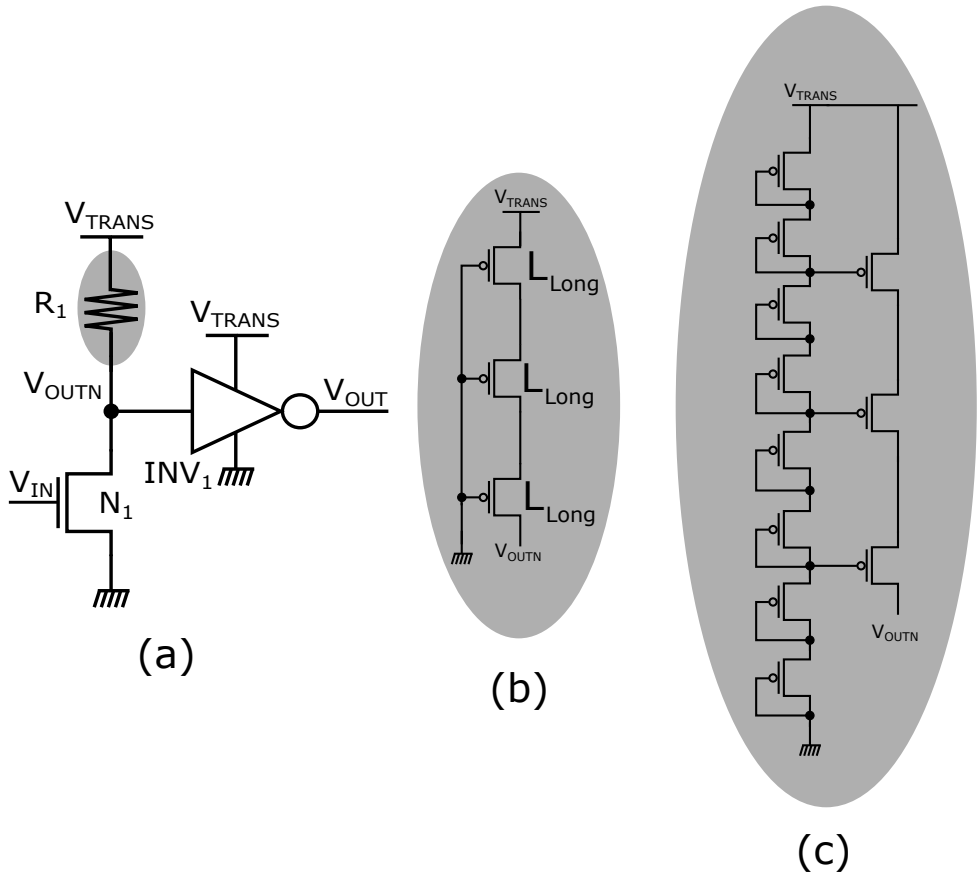


Figure 6.12. The voltage level shifter. (a) The voltage level translation circuit (b) Conventional realization of the large resistor (c) Improved realization of the large resistor

and V_{STOR}. PMOS transistors are used for the design of the power switches because both of the source and drain voltages of switch FET are at supply level. The PMOS pair shown in Figure 6.8 is employed to select the higher voltage of V_{REC} and V_{STOR}. When V_D is high, the gate of the PMOS switch P_{SW} is pulled to ground through the conduction of the NMOS transistor, thus the switch is closed. When V_D is low, the gate of the PMOS switch is pulled to the higher voltage of V_{REC} and V_{STOR}, thus the switch is opened.

When the power switch, P_{SW}, is in ON state, the gate of the PMOS is pulled to ground to conduct current. When it is in OFF state, the gate of the PMOS should be pulled high so that it exhibits very high resistance. However, as a consequence of the two varying supply voltages, we can enter a situation where the source terminal of the PMOS, being connected to the other supply domain, is at a higher voltage potential than the supply voltage that the PMOS switch is controlled by; such a possibility can effectively leave the switch in a partially ON state. However, our smart switch circuit

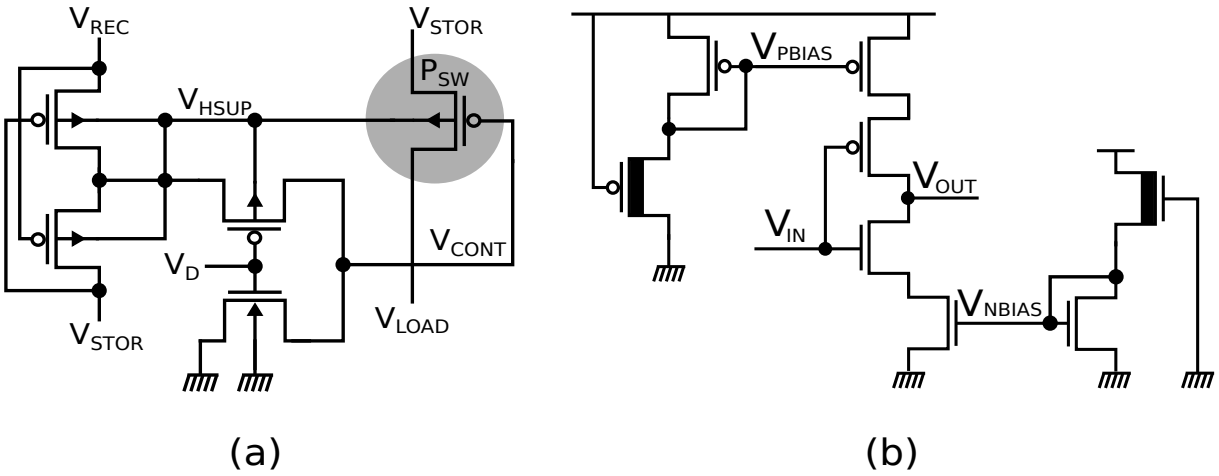


Figure 6.13. The power routing switch and current-starved inverters. (a) The smart PMOS switch is designed to ensure the control voltage V_{CONT} is selected from the higher of the two supply voltages—V_{REC} and V_{STOR}. This switch is employed in the power routing unit, as shown in Figure 6.10 (b) The current starved inverter, used in control unit, also shown in Figure 6.10.

shown in Figure 6.13 (a) is designed to ensure when the gate of the PMOS switch is pulled high, the high signal is emanating from the higher of the two supply voltages, which are V_{REC} and V_{STOR}.

Since the logic circuitry is supplied by the on-chip capacitor at the output of the rectifier, which is in the order of 100 pF, the peak current of the logic circuits has to be minimized. In this work, we used current starved logic as shown in Figure 6.13 (b). The peak current through the inverter is limited by the NMOS and PMOS current sources biased by the NMOS (Figure 6.4(a)) and PMOS 2-T voltage references (Figure 6.4(b)), respectively.

6.5 Simulation Results

The complete HPMU is realized in a GlobalFoundaries 130 nm process and simulations are conducted in Cadence Virtuoso Simulation Environment. We investigate four aspects related to the HPMU: i) power conversion efficiency in the passive and charging mode of operation to understand the amount of excess power that can be directed to a storage element; ii) the power consumption of the HPMU in the various modes of operation; and iii) the transient behaviour of the HPMU under different

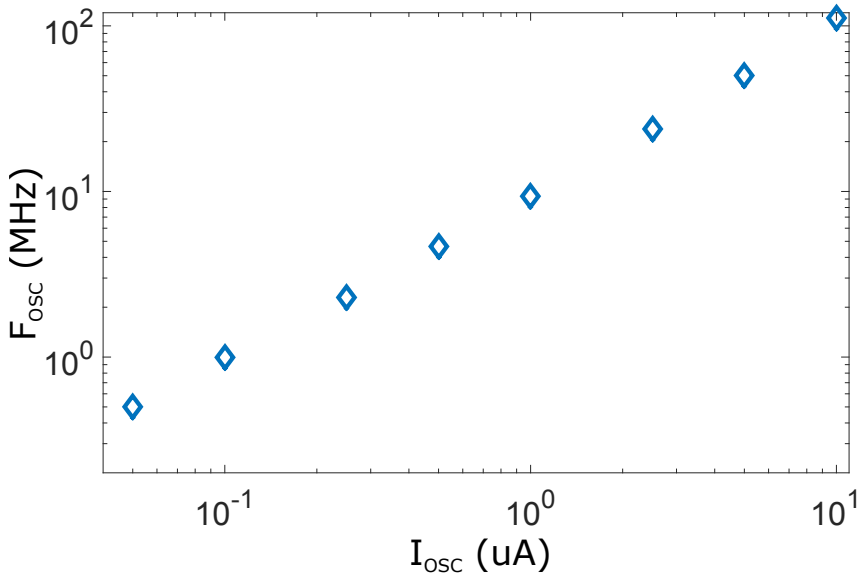


Figure 6.14. The output frequency of the CCO as a function of the current consumed.

operating conditions to verify the active power management capability of the HPMU; iv) cold start-up time comparison between the system with and without HPMU.

The test set-up for the PCE of the charge pump is depicted in Figure 6.15. Here, V_{OSC} is the input to the charge pump, and V_{OUT} is the DC output of the charge pump. Thus, the input power P_{IN} of the charge pump is the product of the input current and V_{OSC} whereas the output power P_{OUT} is then the product of the output current and the voltage V_{OUT}. The PCE of the charge pump in the periodic steady state can be expressed as the following:

$$\text{PCE} = \frac{P_{OUT}}{P_{IN}} \tag{6.1}$$

The oscillator frequency and current consumption of the current controlled oscillator, and the power conversion efficiency (PCE) of the charge pump, are depicted in Figure 6.14 and Figure 6.15 (b), respectively. It can be observed in Figure 6.15 (b) that the optimal PCE (65 %) can be achieved around an output voltage of 2.5 V to 3.5 V, which is the nominal voltage range that the charge pump will operate on during the passive and charging mode of operation. It can also be observed that the PCE does not significantly degrade over the range of operational frequency.

The top-level simulation test bench is shown in Figure 6.16(b). The five-stage differential cross coupled rectifier proposed in chapter 3 is used as the front-end harvester, its output is fed to the input the HPMU. When the rectifier's output voltage

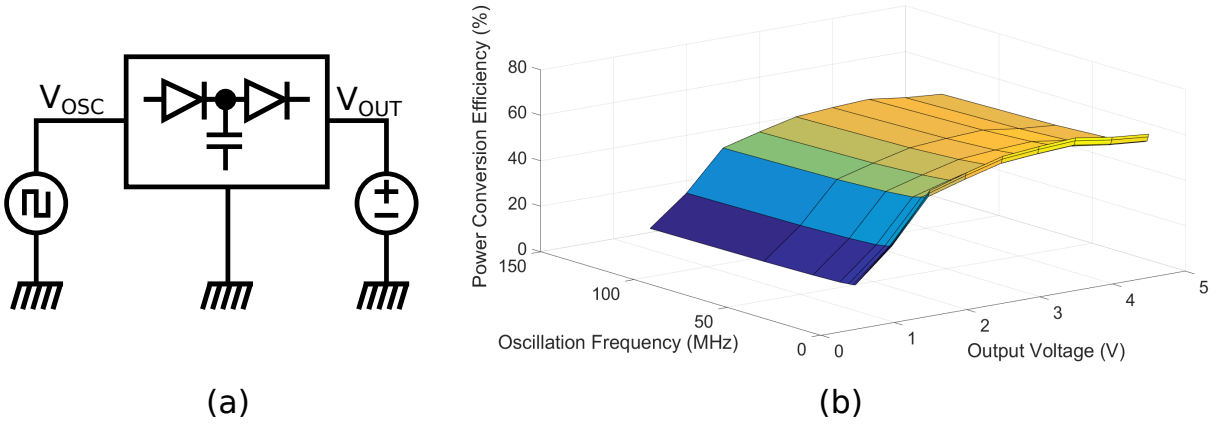
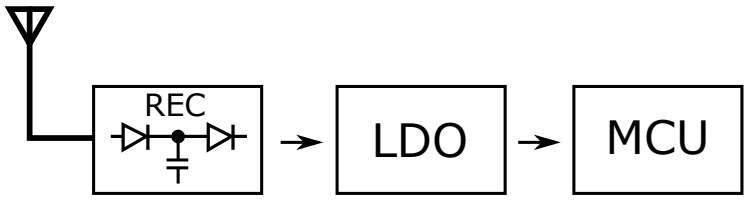


Figure 6.15. Simulation setup and results for the charge pump. (a) The test setup for the measurement of PCE of the charge pump (b) The relationship between the power conversion efficiency (PCE) of the charge pump (CP), oscillator frequency and the output voltage of the charge pump

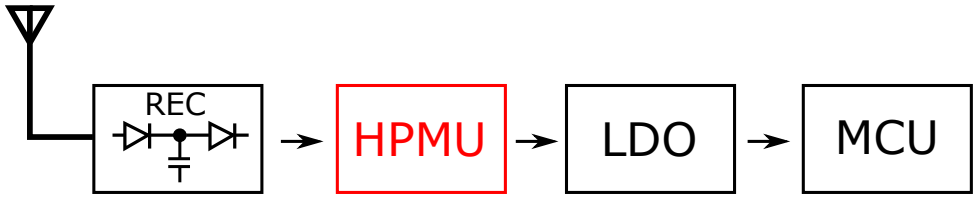
is 2.5 V, the input impedance of its RF port is simulated to be 32 - *j*312 at 915 MHz. Thus, to minimize the interface mismatch, the antenna impedance is set to 32 + *j*312, resulting in optimum overall harvesting efficiency in the passive and charging mode. The differential rectifier has to be driven by a differential antenna, which is not readily available in the circuit simulator. As such, in Figure 6.16 (c), a circuit model, consisting of a port element and ideal balun, is used to emulate the circuit behaviour of a differential antenna.

The power consumption of the HPMU is summarized in Table 6.1. It is worth noting that the CF, CCO and CP do not operate in the semi-passive and off modes. In the passive and charging mode, their power consumption can vary and depends on the excess harvested power. Thus, it is more meaningful to express their power conversion efficiency rather than the absolute power consumption as shown in Figure 6.15 (b). The control logic in the PRU consumes negligible static current, thus after the system enters a state, its power consumption is negligible. When the rectifier's output is 2.5 V, the available current at the rectifier's output V_{REC} is in the order of 100 uA, hence the proposed HPMU poses less than 1 % power overhead.

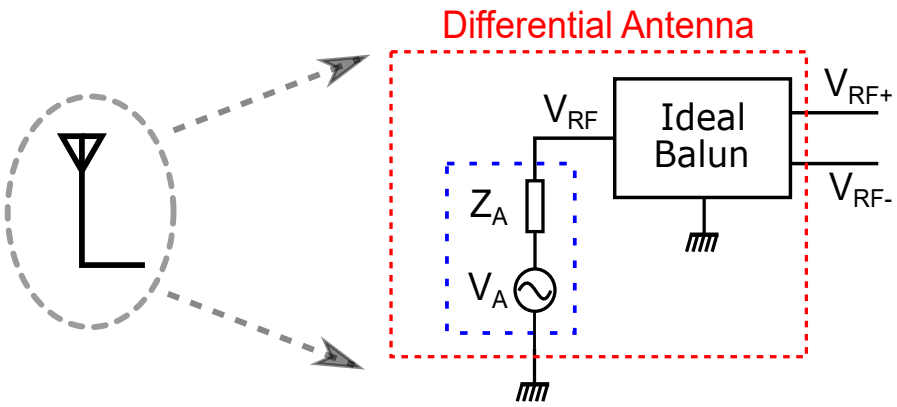
The transient simulation result of the HPMU is shown in Figure 6.17. Here, V_{REC} and V_{STOR} are DC voltage levels of the rectifier's output and the external storage element, respectively. S_{REC} and S_{STOR} indicates whether the rectified power or the power stored in the capacitor is supplying the LDO regulator. The varying V_{REC} is emulated by changing the power level at the input of the rectifier. In addition, in this simulation, the



(a)



(b)



(c)

Figure 6.16. (a) The top-level simulation setup of the system without HPMU (b) with HPMU (c) simulation setup for the differential antenna required by the differential rectifier.

Table 6.1. Power Consumption Summary

Modules	Passive & Charging	Semi-Passive	Off
CF	Variable	N/A	N/A
CCO	Variable	N/A	N/A
CP	Variable	N/A	N/A
1p0Det	10 nW	10 nW	10 nW
2p5Det	2 uW	10 nW	10 nW
StorDet	10 nW	10 nW	10 nW

external storage element is modelled by a 10 nF capacitor to achieve shorter simulation time.

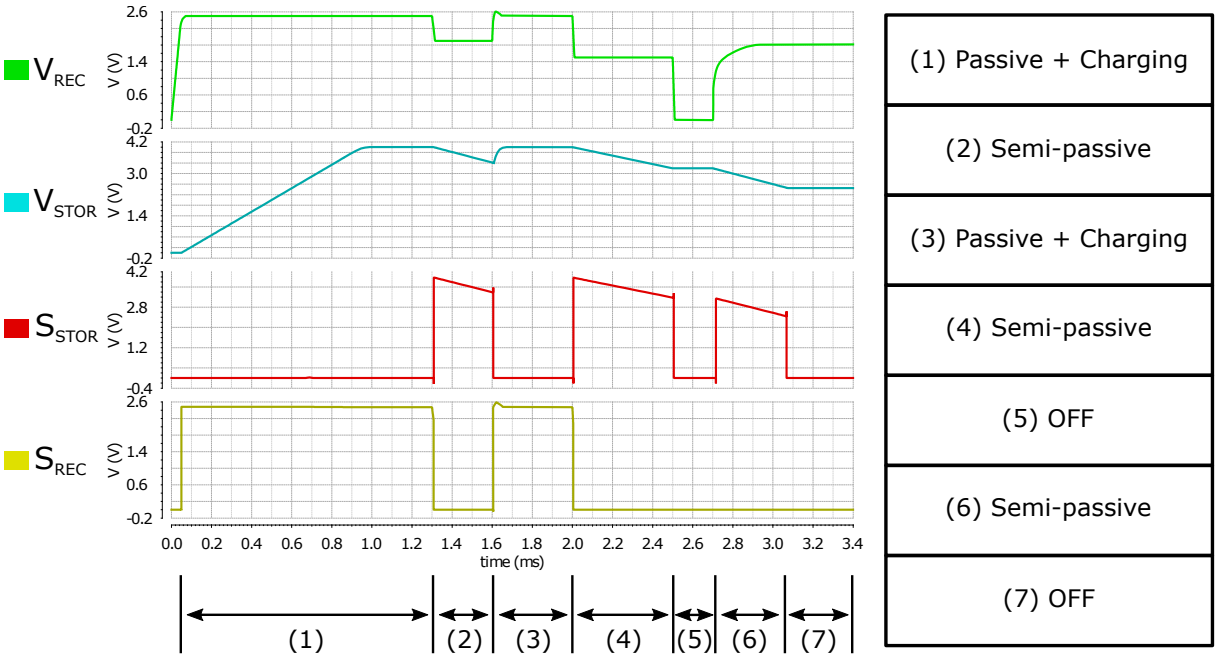


Figure 6.17. System-level simulation to verify behaviour of the HPMU.

To demonstrate that the effectiveness of the proposed HPMU in reducing cold start-up time, the time required for system with—Figure 6.16(b)—and without HPMU—Figure 6.16(a)—at different input power levels are plotted in Figure 6.18. It can be observed that when the input power is very high (e.g. 13 dBm), the start-up time required for both systems are approximately the same. As the input power decreases, the start-up time required for the system without HPMU increases because the energy needed has to be harvested and accumulated over time, thus it is highly dependent on the RF field strength. On the other hand, the HPMU routes power directly from the external energy storage element, thus start-up time is significantly shorter and does not depend on the input power level. As discussed previously, systems without HPMU requires V_{REC} of 2.5 V for start-up whereas systems with HPMU only requires 1 V, corresponding to input power levels of -5 dBm and -29 dBm respectively. Hence, the HPMU dramatically improves the input power sensitivity of the overall system.

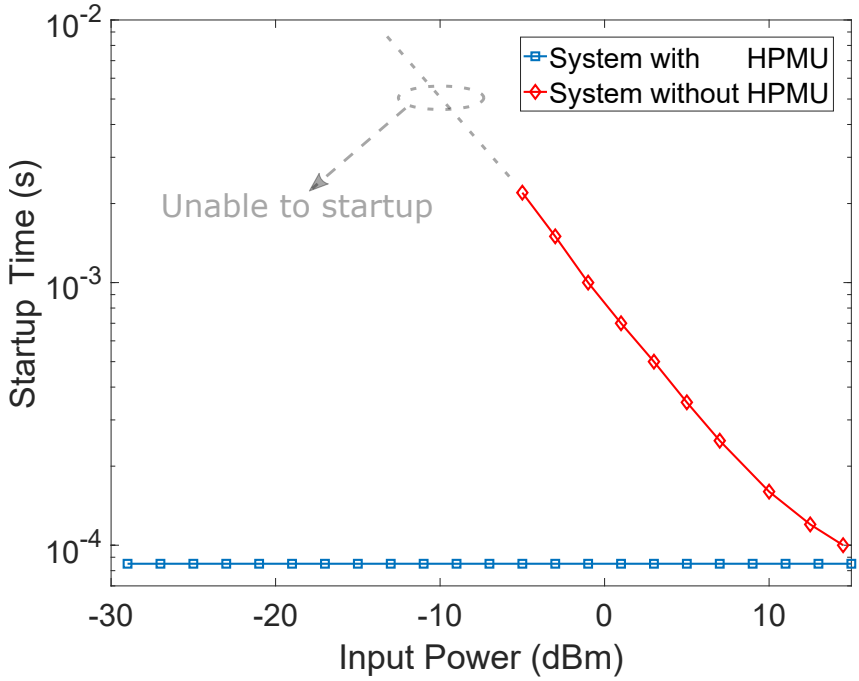


Figure 6.18. Cold start-up times for systems with and without HPMU at different input power levels.

6.6 Related Works

Achieving reliable operation of passive devices, including sensor enabled RFID tags, have exploited other approaches such as the integration of alternative ambient sources of power such as solar power to accompany the harvested RF power to realize hybrid powering schemes (Sample et al., 2011; Lemey et al., 2016) or the use of multi-band power harvesters (Parks et al., 2014). Such approaches also provide an effective approach to the problems we have considered with the added requirement of integrating additional mechanisms on passive devices such as solar panels, relatively large wide-band antennas and additional hardware including multiple rectifiers and power summations stages to capture ambient power.

Charge burst schemes are another well-established approach to harvest power (Umeda et al., 2006; Papotto et al., 2014; Michelon et al., 2016) and they typically involve collecting charge over time in the "charge phase" and subsequent use of this energy to supply the system in a significantly shorter "burst phase", to potentially extend operational range. However, performance and responsiveness of applications built on such approaches are sacrificed due to the long "charge phase" are still subjected to the indeterministic nature of RF power harvesters as highlighted in (Parks et al., 2014; Sample et al., 2011; Lemey et al., 2016).

A related design for power routing is offered in the Enerchip CC from Cymbet (Cymbetcorp, 2012) and was employed in (Dong et al., 2015) to realize the proof of concept hybrid power management unit. However, Enerchip CC makes its power routing decisions in response to only one threshold voltage level. More importantly, the key differences that sets this work apart from Enerchip CC are: i) the proposed approach attempts to convert all of the excess energy by pulling as much current as necessary from rectifier's output while regulating this voltage at a defined threshold; and ii) Enerchip CC consumes significantly higher amounts of power to realize its power routing functions.

To the best of our knowledge, there are no existing integrated solutions in the literature for actively managing harvested power of passive RFID tags by storing and intelligently routing power as proposed in this study to overcome brownouts, cold-start problems and achieve a highly responsive tag platforms to support emerging applications looking to integrate not only identification but sensing capability to passive RFID tags. Further, our proposed architecture can be integrated to actively manage other ambient sources of power such as solar and customized to suit the needs of target device platforms.

6.7 Conclusion and Discussion

This chapter presents a fully-integrated hybrid power management unit for the UHF energy harvester, in the context of UHF RFID. The presented design is unique in that it actively manages the harvested power to reduce brownout events, shorten cold start-up times and extend operational range as well as realize more responsive tags, especially those requiring higher power due to integrated sensors. The design was demonstrated and validated through simulation-based experiments in Cadence Virtuoso Design Environment and the results showed that the proposed design converts and stores excess power with very high efficiency and consumes negligible power compared to the available power at the rectifier's output.

Throughout Chapter 2 to Chapter 6, we have developed a solid understanding of UHF energy harvesting and power management. In the next, we develop an energy harvesting system to with the aim of reaching an input power sensitivity as low as -40 dBm.

Chapter 7

Ultra-low-power UHF energy harvester with input power sensitivity of -40 dBm

THIS chapter presents the design of an ultra-sensitive UHF energy harvester operating at 915 MHz. The design is able to develop 1.5 V output voltage when an input power of -40 dBm is applied from a standard 50 Ohm interface. The design consists of mainly three important building blocks. First, a 5-stage front-end rectifier is used to rectify the input RF power into DC voltage of roughly 100 mV. Then, an ultra-low-voltage charge pump is employed to boost this 100 mV to 1.5 V. Finally, an ultra-low-power control unit is designed to coordinate the charge-burst action between the front-end RF rectifier and charge pump to develop the final harvester DC output.

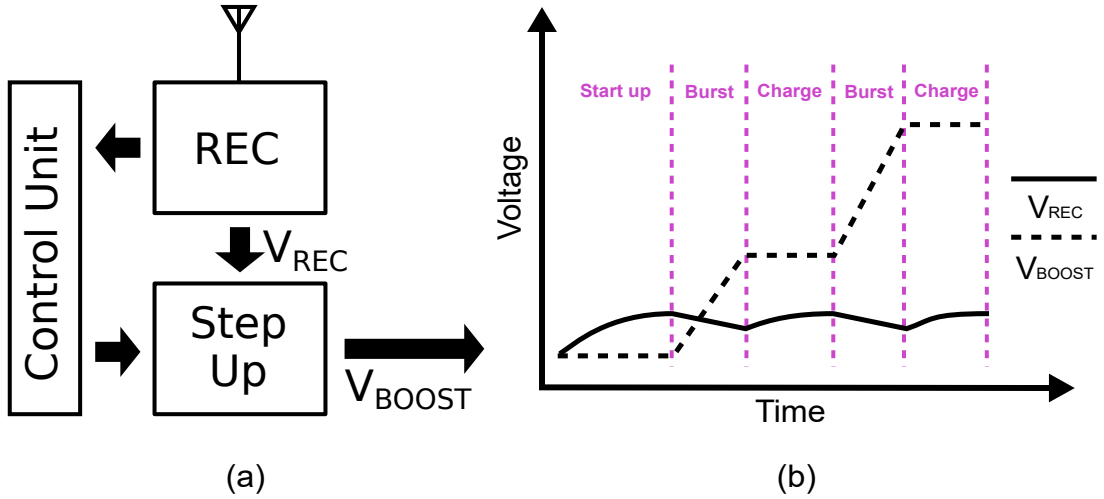


Figure 7.1. The complete charge-burst harvester. (a) An block diagram overview of the complete harvester to be presented in this chapter (b) A graph that illustrates the charge-burst action in the harvester

7.1 Introduction

In this chapter, we will present a UHF harvester design that is capable of developing more than 1 V at −40 dBm input RF power. This harvester consists of a highly-sensitive front-end RF rectifier which converts the RF input voltage to DC, a second-stage charge-pump that boosts this intermediate DC voltage to 1.5 V, and finally a control unit that controls the charge pump and the rectifier to develop the final 1.5 V, in a charge-burst manner. The block diagram overview of the design is depicted in Figure 7.1 (a). The front-end RF rectifier develops an intermediate voltage called V_{REC}, which is initially 0 V. When V_{REC} reaches a pre-defined activation voltage level, the step-up converter is activated to up-convert V_{REC}, to the output voltage of the step-up converter, V_{BOOST}. At −40 dBm, the power consumed by the step-up converter will be substantially more than the power harvested. Therefore, the V_{REC} will drop very quickly during the burst phase and when it falls below the pre-defined de-activation threshold, the step converter is disabled, and the system returns to charge phase. This charge-burst process is depicted in Figure 7.1 (b).

7.2 RF front-end harvester

In this section, we discuss the design of the front-end harvester. The goal of the design is to achieve more than 0.1 V DC rectifier output voltage at input power of −40 dBm.

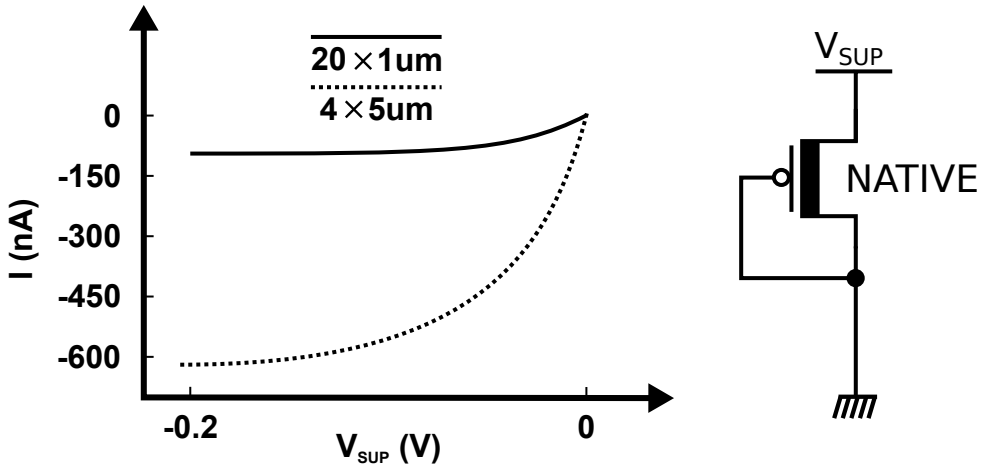


Figure 7.2. Comparison of transistor dimensions. 20 × 1 μm (L × W) configuration is chosen over 4 × 5 μm configuration due to less reverse leakage current.

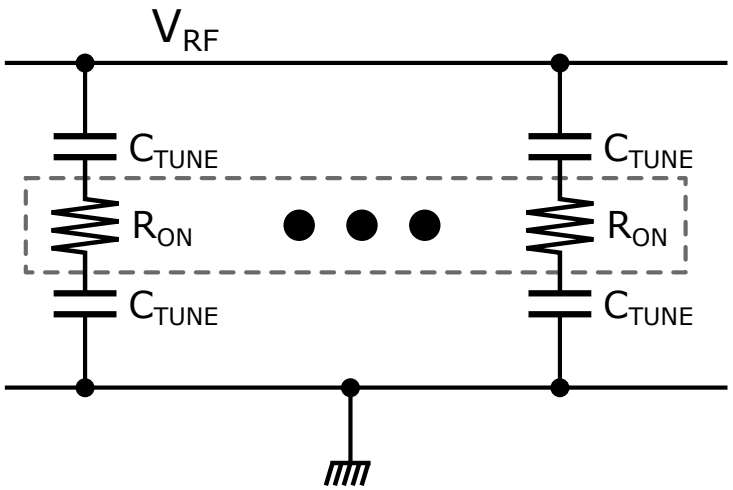


Figure 7.3. On-state resistance of switch-able capacitor banks. a problem with the design in (Stoopman et al., 2014)

Therefore, the high sensitivity is prioritized over PCE at moderate input power levels. With this goal in mind, a 5-stage classical single-ended Dickson charge-pump topology was designed to produce a DC voltage of more than 100 mV at -40 dBm input power, as shown in Figure 7.4. Native transistors, which exhibit near-zero threshold voltage, are employed for the design of front-end RF rectifier. The chosen thick-oxide native transistor was dimensioned to have 20 fingers with 1 μm finger width and 1.4 μm length (minimum), this is done to achieve smaller reverse leakage current and better RF performance (smaller parasitic capacitance). The size of the RF coupling capacitor is 1.2 pF and the DC load capacitor is 4.5 pF. The matching network in (Oh et al., 2012) is employed, because in this design we prioritize input power sensitivity over maximum

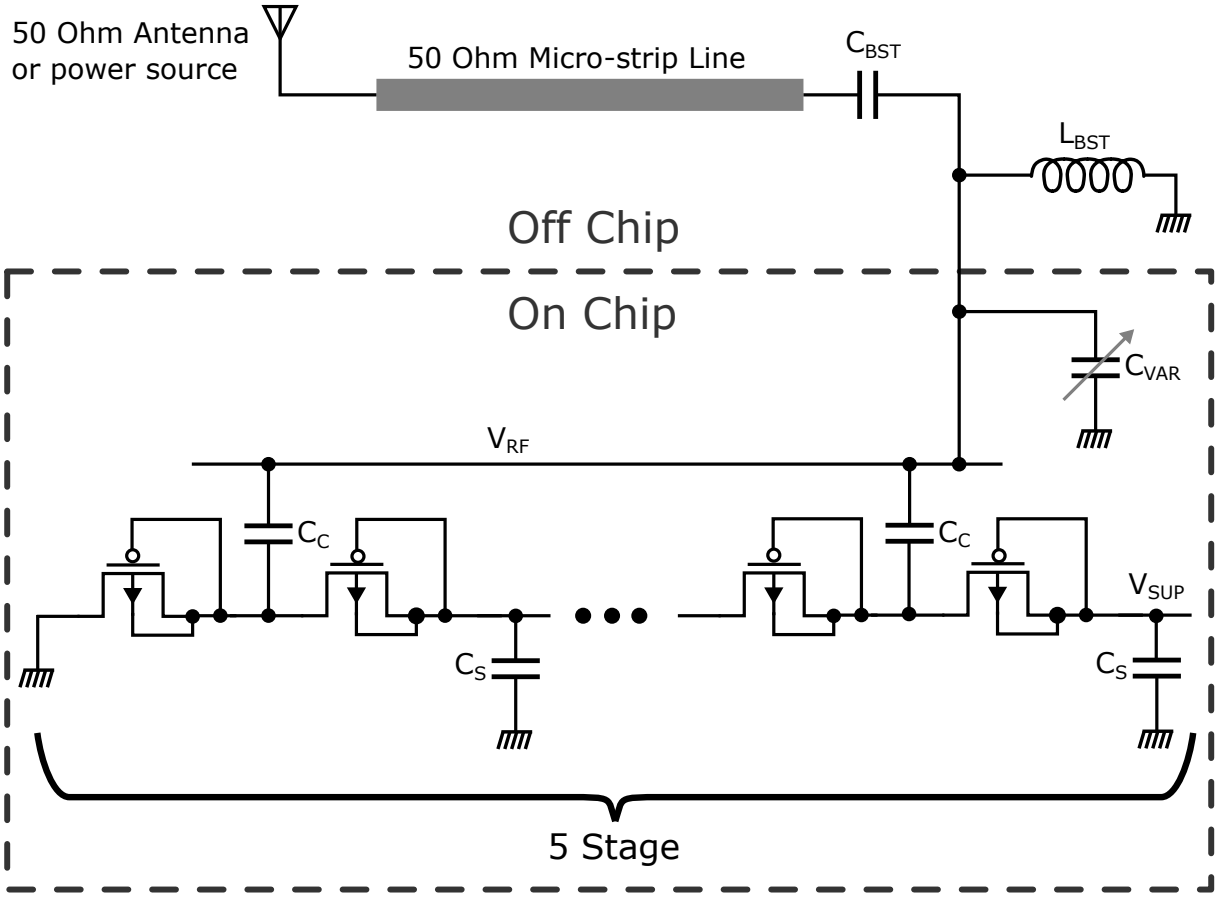


Figure 7.4. The overall block diagram of the front-end RF energy harvester.

overall PCE, and also because we aim to drive the rectifier from a standard 50 Ω source impedance.

The passive booster, as shown in Figure 7.4, consists of a serially connected capacitor C_{BST} and a shunt inductor L_{BST}. These two components of the passive booster already provide two degrees of freedom for optimizing the voltage boosting. However, passive components typically come in discrete values. For example, inductors tend to vary by 1 nH or more and capacitors tend to vary by 50 fF. With only two degrees of freedom for tuning, it might not be always possible to achieve the most optimal passive boosting. In (Stoopman et al., 2014), a bank of switch-able capacitors are added in parallel to the RF input, this way, the optimal capacitance from the RF input to ground can be achieved. However, when the input power is as low as -40 dBm, the on-state resistance of the RF switches consumes a substantial proportion of the power which worsens the input sensitivity, as shown in Figure 7.3. To that end, a varactor was added from the

RF input to ground, which not only eliminating the on-resistance, but also provides a continuous variation of the capacitance from RF input to ground.

The entire front-end RF harvester is depicted in Figure 7.4. Together with the main 5-stage rectifier, the varactor is also placed on the RF line. The RF signal then continues off chip, the passive booster, consisting of C_{BST} and L_{BST}, is placed as close to chip input as physically possible to avoid discontinuity due to distributed effects. The two components within the passive booster vary from 20 nH to 30 nH and 100 fF to 500 fF, respectively. To obtain excellent distributed effects, the gap between the passive booster and the 50 ohm antenna (or any other 50 ohm input power source) is bridged using a 50 ohm micro-strip line.

7.3 The Control Unit

For the charge-burst cycle to be executed in an orderly manner, a control unit is needed to turn on and off the charge pump at appropriate instances. In addition to this, switches at the input and output ports of the charge pump are required to ensure that, during the charging phase, the charge pump is not loading the front-end RF harvester and charges already pumped into the output capacitor is not flowing back into the charge pump. The overall block diagram of the control unit is depicted in Figure 7.5. The operational principle of the control unit is described as follows: The system starts up in charging phase, the output of the voltage detector VDET is low and the inverting level shifter pulls its output to V_{SUPH}. During the charging phase, the output of the main rectifier V_{SUP} rises progressively and eventually reaches the pre-defined rising threshold. When this occurs, the voltage detector pulls its output to V_{SUP} and subsequently the level shifter, LVLSHIFT, pulls its output to ground.

7.3.1 The Auxiliary Rectifier

An auxiliary rectifier is employed to develop a near open-circuit voltage that is higher than V_{SUP}. Thus, we call it V_{SUPH}. The auxiliary rectifier also employs the Dickson charge pump topology and is used in conjunction with the main rectifier, however, the transistor types and dimensions used are drastically different from those in the main charge pump. To avoid substantially affecting the input impedance behaviour of the main rectifier, the auxiliary rectifier has been designed with thin oxide native

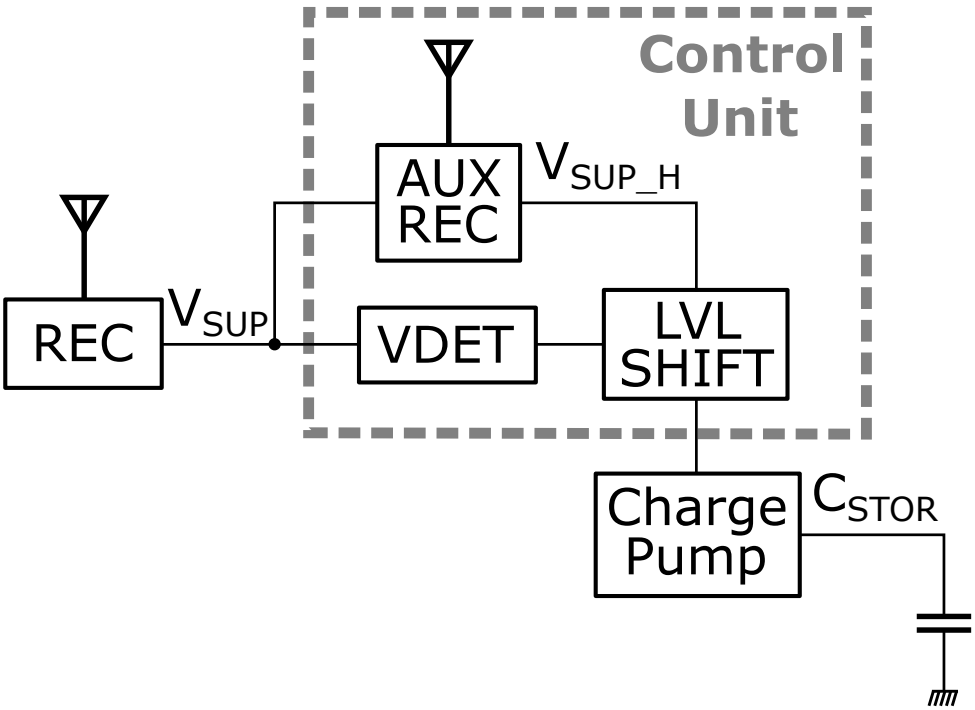


Figure 7.5. A block diagram overview of the control unit. The unit consists of an auxiliary rectifier, a voltage detector, voltage level shift, and an input and output switches for the charge pump.

transistors with minimum length and width. In addition, 150 fF MIMCAPs were used as coupling capacitors to further minimize the influence of the auxiliary rectifier over the performance of the main rectifier.

7.3.2 The Voltage Detector (VDET) and the Voltage Level Shifter (LVL-SHIFT)

The voltage detector needs to pull its output voltage to V_{SUP} when V_{SUP} exceeds 130 mV and to ground when V_{SUP} falls below 110 mV, thus providing roughly 20 mV worth of hysteresis. Schmitt trigger is one of the classical approaches for providing hysteresis. However, as discussed in (Goeppert et al., 2016), the hysteresis of Schmitt trigger diminishes when the supply voltage approaches ultra-low voltages such as 100 mV or lower.

In this work, instead of the Schmitt trigger, an amplifier with ratioed input devices was used, as shown in Figure 7.6. Conventionally, with this topology, the gate terminal of one side of the input transistor is tied to the supply voltage and the other to ground. And, the side that is tied to ground is often wider than the side that is tied to the supply

voltage. Therefore, initially the supply voltage is low, the output of the amplifier is pulled to ground by the side of the input transistor whose gate terminal is tied to ground. When the supply voltage reaches the value when the thinner transistor is able to pull roughly the same level of current, the output voltage is somewhere between the supply voltage and ground. Eventually, when the supply voltage is so high that the thinner input device pulls significantly more current than the wider input device, the output is pulled to the supply voltage. Adding an extra input device on the left side (connecting its gate terminal to the "en") does not help, because although this will left-shift the down-sweep edge but also left-shift the up-sweep edge as well. Therefore, in the end, hysteresis remains unchanged. If we add an extra input device on the right side (connecting its gate terminal to the "enb"), this will right-shift up-sweep edge but keep the down-sweep edge still, enlarging the hysteresis. However, this is at the cost of increasing the minimum turn-on voltage.

To mitigate these issues, the back-gate terminal of the wider transistor was exploited and is connected to "enb". It initially reduces the threshold voltage of the wider transistor when the output "en" is low ("enb" is high), then increases the threshold voltage of the wider transistor when output "en" is high ("enb" is low). This approach is effective in creating the hysteresis without increasing the minimum turn-on voltage. Since the supply voltage during operation is very low, tying the back-gate to the supply terminal is safe.

For the voltage level shifter, the single-stage OTA was utilized again. As shown in Figure 7.7, the gate terminal of the wider input device is once again tied to ground and the gate terminal of the thinner input device is tied to the output "en" from the voltage detector. This way, when the supply voltage passes the detection level, "en" is pulled to its supply voltage and the output level shift is pulled to ground. Before supply voltage reaches the detection level, the "en" from the voltage detector is zero and the wider input device pulls more current than the thinner input device, the output is pulled to its supply voltage, which in this case is V_{SUPH}. The ratioed input devices prevent the voltage level shifter from being false-triggered by the initial start-up bump in the "en" output signal, which is inevitable.

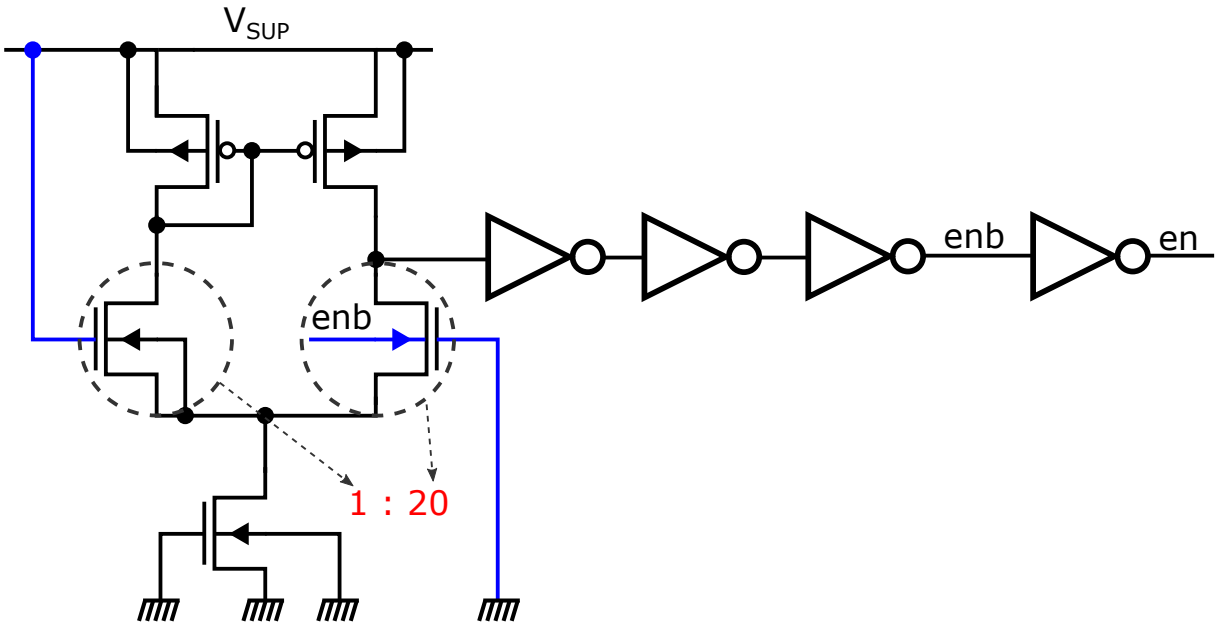


Figure 7.6. Achieving hysteresis with ultra-low supply voltage.

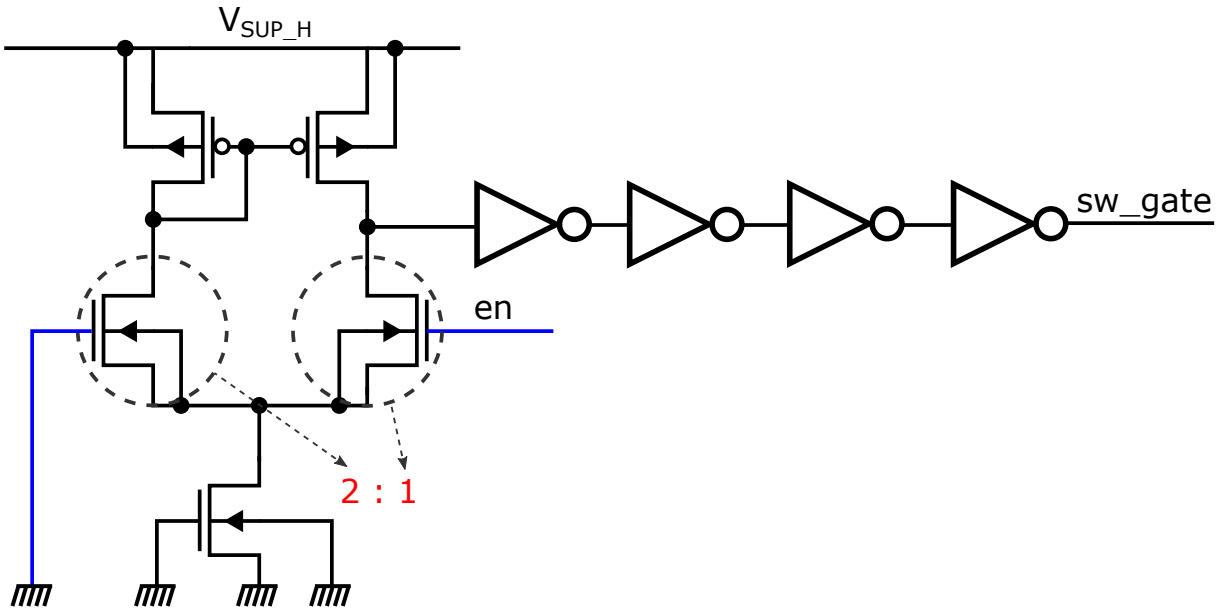


Figure 7.7. The voltage Level Shift.

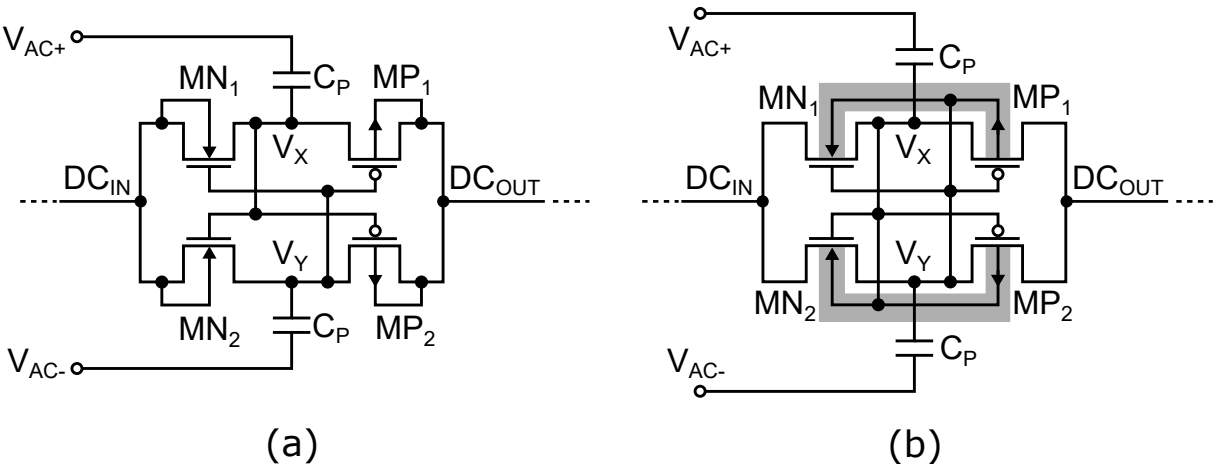


Figure 7.8. Differential-drive threshold compensation techniques (a) conventional approach (b) improved approach.

7.4 Ultra-low-voltage Charge Pump

In this work, the front-end UHF harvester develops 0.1 V, then a step-up converter is required to boost the 100 mV to more than 1 V. In the literature, substantial efforts have been made to development of ultra-low voltage step-up converters. (Ramadass et al., 2010) designed a step-up converter with a nominal operating input voltage of 35 mV, which uses 3 external inductors and 1 V of pre-charge voltage. (Carlson et al., 2010) designed a step-up converter which operates off the 20 mV input voltage, however the design requires an external inductor and a pre-charge voltage of 600 mV. These two designs both require a pre-charge voltage which is an order of magnitude higher than the operating input voltage. An energy harvester converts power and develops an output voltage from its input and the most important criteria of the harvester is that it needs to be self-sustaining, thus a pre-charge voltage an order of magnitude higher than the input operating voltage is unacceptable for energy harvesting and subsequently these two designs are not suitable for our proposed architecture. (Michelon et al., 2016) designed a step-up converter that requires an operating input voltage of at least 200 mV, which is almost twice as much as specified in our application. (Goeppert et al., 2016) and (Fuketa et al., 2017) designed a step-up converter that requires 100 mV or less, however both of these designs entail a sluggish start-up phase in order of a second, which our harvester design cannot tolerate because burst period is very short. (Guler et al., 2014) designed a step-up converter with 85 mV operating input voltage, however it requires an on-chip transformer, resulting

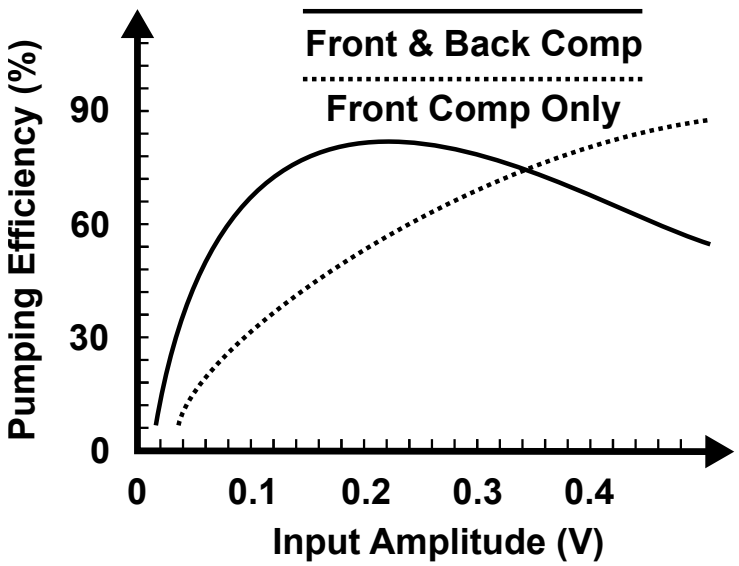


Figure 7.9. Comparison of the pumping efficiency of the two differential-drive charge pumps stages.

in a chip area of 1.8 mm^2 for the whole design, which is against the economical and cost-effective nature of the energy harvesting and IoT chips. In this work, we designed an area-efficient and ultra-low voltage charge pump.

7.4.1 Back-gate compensated charge pump stages

It is well understood in the literature that a cross-coupled inverter-based charge pump stages are very efficient for small input AC amplitude, as depicted in Figure 7.8 (a). The opposing V_X and V_Y act as dynamic threshold compensating voltages for the upper and lower side of the charge pump. When V_X is positive, the device MN_1 shuts off and MP_1 conducts. On the other hand, when V_Y is negative, which further shuts off MN_1 and boosts the conduction in MP_1. In this work, due to the availability of deep-nwell options, the bulk terminal was tied to its gate terminal to achieve dynamic threshold compensation, as depicted in Figure 7.8 (b). When the V_X is positive, V_Y is negative which increases threshold voltage of MN_1 and reduces the threshold voltage of MP_1, which further improves the conduction and shut-down behaviour of the MP_1 and MN_1, respectively.

Compared to the circuit in Figure 7.8 (a), the dynamic approach achieves better pumping efficiency (i.e. V_{OUT}/V_{IN}) at lower AC input voltage amplitude. This is demonstrated in Figure 7.9. It can be observed that, from 0 to 0.3 V, the charge pump with both front and back-gate compensation achieves significantly

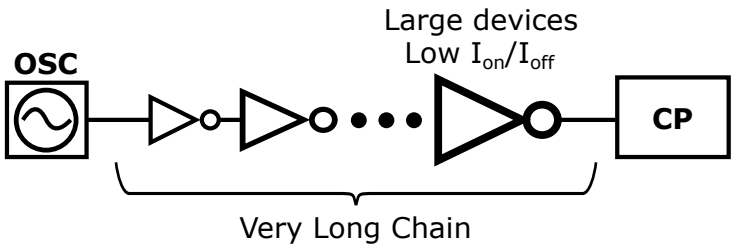


Figure 7.10. Huge Buffers needed for sub-100 mV operation due to limited Ion and Ioff ratio, resulting in a very long buffer chain.

better pumping efficiency than the charge pump with only front gate threshold compensation. However, after the input AC amplitude passes 0.3 V, the design with back-gate connection has more reverse leakage for the same level of common-mode compensating voltage. As a result, the pumping efficiency of the design where both front and back gate are compensated dropped below that of the design with only front-gate compensation.

7.4.2 Self-oscillating Buffers (SOB)

The conventional approach to the design of charge pump drivers relies on an inverter chain to gradually build up the drive strength from the output of an oscillator, as depicted in Figure 7.10. With a supply voltage of 100 mV or less, I_{ON}/I_{OFF} is very small. The size of the final stage charge pump driver needs to be excessively large to provide sharp transition edges at the input of the charge pump stages. At nominal supply voltages, a size increase of 4X is typically used for the inverter chain that is used to build up the drive strength. However, this is not case for extreme low supply voltages, such as 100 mV or lower. The current that is used to charge and discharge the next stage inverter is essentially the difference between I_{ON} and I_{OFF}. When I_{OFF} becomes a noticeable percentage of the I_{ON}, this difference becomes significantly smaller and could be insufficient to drive the next stage inverter at a specified speed. Therefore, the increase in size in the inverter chain has to be adjusted at a much more gradual pace. As a result, the inverter chain can be exceedingly long, which is extremely wasteful in terms of power consumption and chip area.

In this work, instead of using invert chain, we configure the buffers in a loop, thus they self-oscillate. As depicted in Figure 7.11 (a), the buffers are put in two loops, each consists of three buffers to provide the sufficient phase shift for sustained oscillation. In addition to these two loops, cross-coupled inverters are inserted between the output

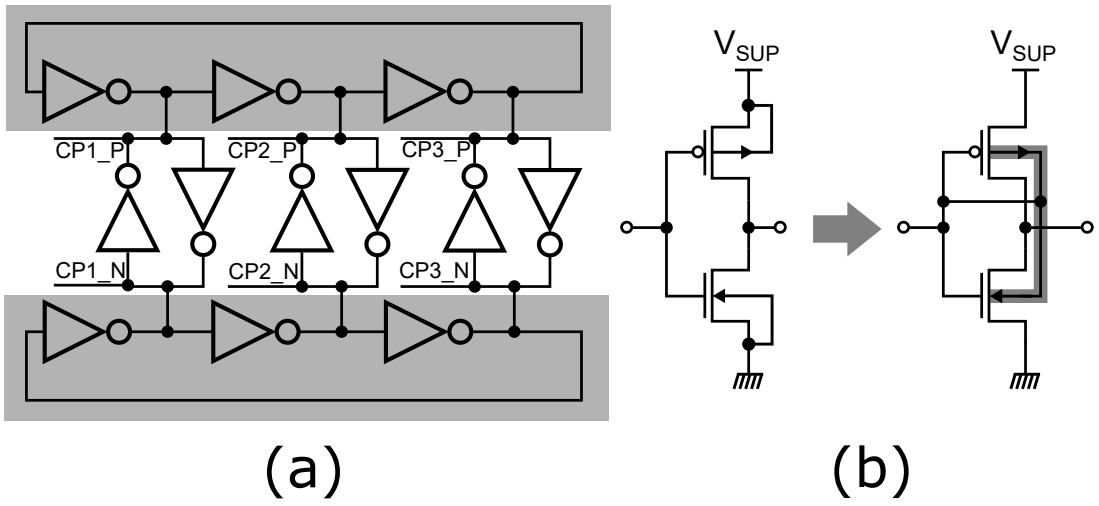


Figure 7.11. The self-oscillating buffer (SOB). (a) Self-oscillating buffer chain (b) inverters employ the dynamic threshold compensation by tying the bulk terminal back to its own gate

of each buffer in each loop, as shown in Figure 7.11 (a). The overall topology can be recognized as high frequency differential ring oscillator, where the cross-coupled inverters are used to provide differential output signals and these latches are sized to much smaller than the inverters in the upper and lower inverter loops. In this work, however, in addition to providing the phase shift, the latches are also used to provide sharp edges. The positive feedback inherent of the cross-coupled inverters accelerate the transition from low to high state, and from high-to-low state, thus these latches need to be sized similarly with the inverter buffers in the two loops. All inverters employ dynamic threshold compensation techniques by tying the bulk terminal to the gate terminal and as shown in Figure 7.11 (b) when the gate voltage is high, the bottom NMOS transistor conducts and its threshold voltage is reduced because the bulk terminal voltage is high, on the other hand, the top PMOS transistor shuts down and its threshold voltage is nominal due to the high bulk terminal voltage. In this design, all transistors, including those in inverters and latches, are driving the charge pump stages directly, thus there are no superfluous transistors.

The self-oscillating buffers generates 3 pairs of differential outputs, with 60 degrees phase in between. Each pair of differential outputs drives 20 serially connected charge pump stages and the 3 branches of 20 charge pump stages are configured in parallel to produce the DC output voltage V_{BOOST}, as shown in Figure 7.12. Each single-stage charge pump has two 500 fF pumping capacitors, which results in a total of 60 pF capacitance in the whole charge pump array. The multi-phase nature of the clocking schemes helps reduce the output ripple for a given capacitor size

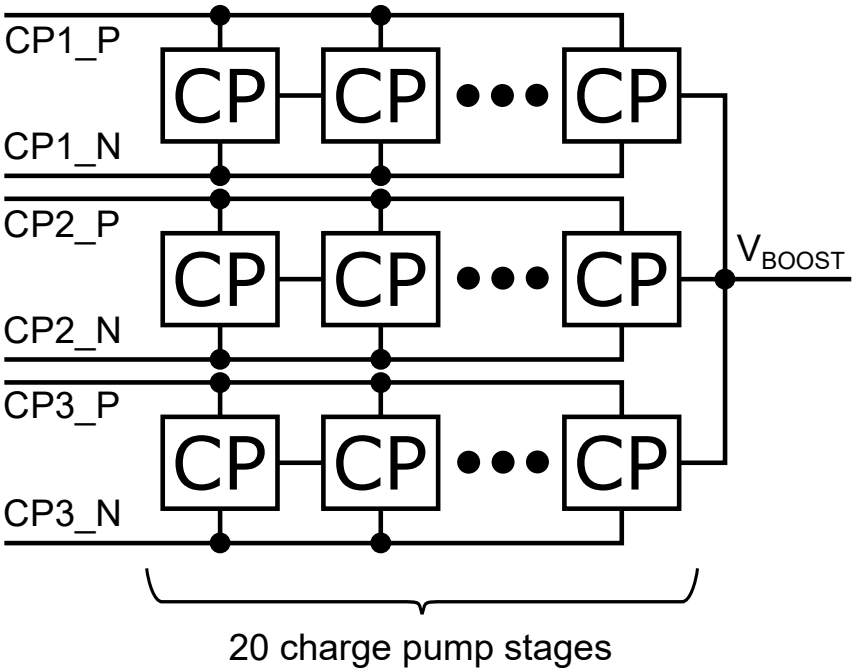


Figure 7.12. The SOB drives 20 by 3 charge pump stages .

and it also help reduce the size of the individual inverter buffer, which eliminates the unnecessary self-loading and leakage current. With 100 mV input voltage, the designed self-oscillating buffer, loaded by the 60 charge pump stages (Figure 7.12), is able to oscillate at 100 kHz. The signal transition period is less than 5% of the overall clock period.

7.4.3 Input and output switches for the charge pump

At -40 dBm input RF power, the output power of the front-end harvester is tiny. As a result, the period of the charge-burst action is very long, can be in the order of a second. During charging, we need to make sure that no current is leaked into the charge pump, so that the output of the RF front-end rectifier is not loaded by the charge pump. However, in ultra-low voltage operations (100 mV or less), it is very hard to implement switches, due to the limited I_{ON}/I_{OFF} ratio. In this work, the negative V_{GS} bias the native transistor is exploited to implement the input switch under this extremely low supply voltage. As shown in Figure 7.13, a 5 V native PMOS transistor is used to implement this switch. When the output V_{RECT} is below the threshold of the voltage detector, the output of V_{DET} is low and the output of the voltage level shift is high, which is V_{SUPH} in this case. Both the back-gate and front-gate of the PMOS

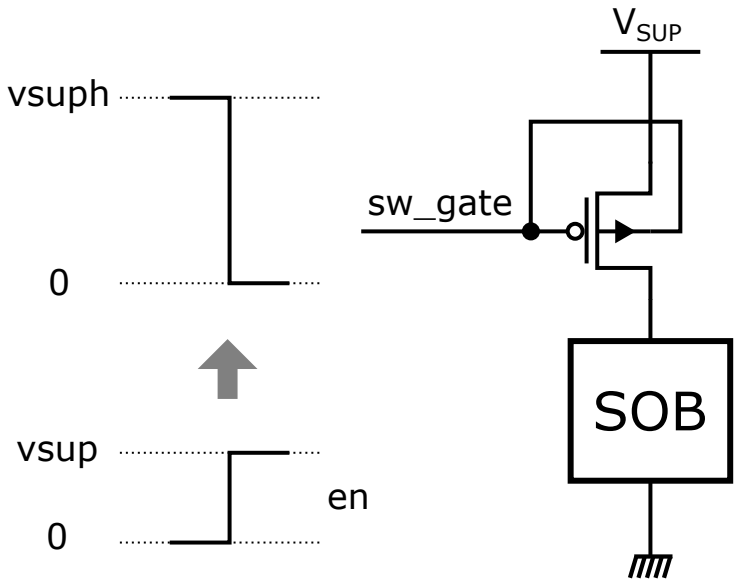


Figure 7.13. Input switch of the charge pump to prevent loading of the RF rectifier during charging phase.

transistor are tied to the output of the voltage level shift, and they are at a higher voltage potential than its source, which is at V_{SUP}. As a result, the V_{GS} of the PMOS transistor becomes reverse biased and the threshold voltage increases, the leakage current becomes extremely small, as a result. When V_{RECT} exceeds the threshold of the voltage detector, the output of the voltage detector "en" is pulled high to V_{SUP}, and the output of the level shift is subsequently pulled to ground. The V_{GS} of the transistor becomes forward-biased and is roughly 100 mV at -40 dBm input power. The critical element of the design is that the threshold voltage, which in this case is close to zero, has to be placed in the middle of the switch input voltage range. This is to ensure that we can achieve the highest I_{ON}/I_{OFF} for our limited voltage headroom.

Due to the slow charging phase when the input power is -40 dBm, it is also necessary to design an output switch for the charge pump that conducts during burst phase and shuts off during the charging phase. This is to ensure that the charge already transferred to the output storage capacitor is not leaked back into the charge pump during the slow charging phase. Conventionally, the simplest way to achieve this to add a diode at the output. In CMOS, to implement the diode we can either use diode-connected transistor (7.14 (a)) or a complimentary MOS transistors (7.14 (b)).

The complimentary MOS diode is often considered superior to the diode-connected transistor because of its lower leakage when the reverse bias voltage is high. However, with moderate reverse bias voltage (around the threshold voltage of the transistor),

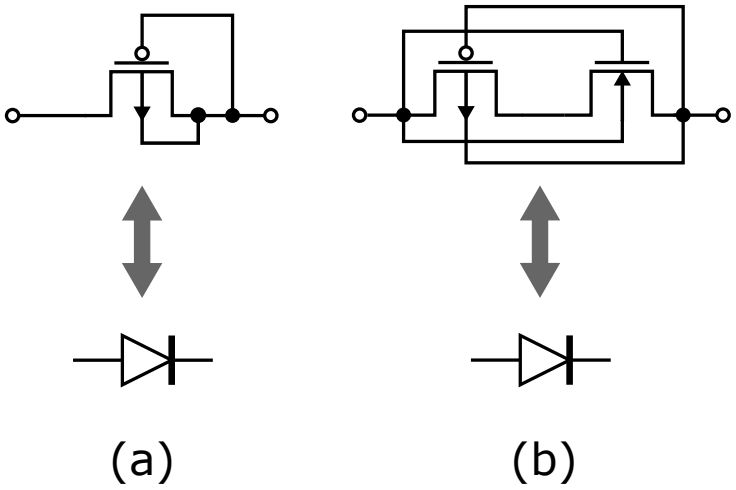


Figure 7.14. (a) The simple diode connected transistor (b) The CMOS complementary diode.

the leakage current is similar to that of the reverse-biased diode-connected transistor. When forward biased, the conduction current of the complementary diode is similar to diode-connected transistor, depending on the threshold voltage of the transistors. In this work, we proposed a hybrid active diode, as shown in Figure 7.15. In this design, the PMOS is 5 V native transistor whereas the NMOS device is 1.5 V standard-V_{TH} transistor. When the system is in burst phase, both the main charge pump and the auxiliary charge pump are active, the auxiliary charge pump develops a positive V_{GS} bias for the NMOS transistor to offset its threshold voltage. The effective voltage drop across this active diode in the burst phase is practically zero. In the charging phase, the self-oscillating buffer (SOB) is disabled and a switch is employed to short the gate terminal of the NMOS transistor to ground to ensure extreme low leakage current even with moderate reverse bias voltage. Hence, we obtain an active diode that has a negligible turn-on voltage when forward biased, and superior leakage reduction for all reverse bias voltages. An auxiliary charge pump stages are designed to boost the gate voltage of the NMOS transistor and minimum size transistors are used in these charge pump stages to prevent overloading of the self-oscillating buffer.

7.5 Simulation

7.5.1 Full transistor level simulation

For the simulation, because the power consumed by the charge pump is orders of magnitude higher than the power harvested from the RF rectifier, a 1 uF capacitor is

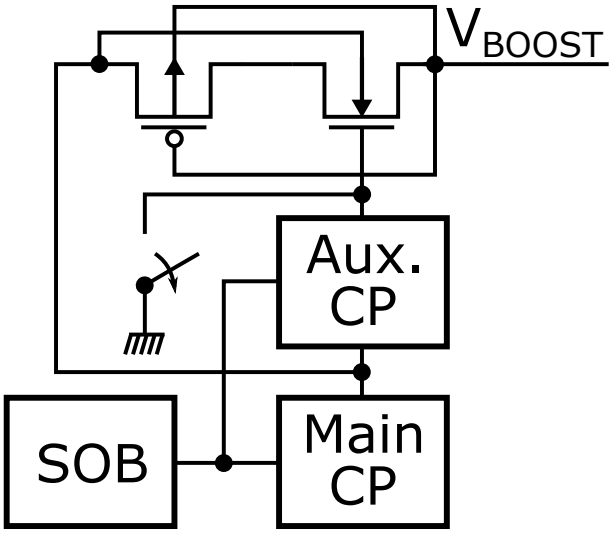


Figure 7.15. A hybrid complementary diode.

placed at the output of the main rectifier, V_{SUP}. Because the current capability of the auxiliary rectifier stages is very weak, thus 500 pF capacitor is placed at the output of the auxiliary rectifier V_{SUPH} to deal with the sudden transient current of the voltage level shift. With this capacitor configuration and an input power of -40 dBm, the charge-burst period is extremely slow which can be in the order of 100s ms or even seconds. With an input frequency of 915 MHz, and due to the ultra-low-power nature of the simulation, the simulation has to be conducted in a relatively high accuracy mode.

To that end, the Advanced Parallel Simulation (APS) option of the Cadence Spectre simulator was exploited, this option substantially accelerates the transient simulation and takes advantage of the multi-threading capability of modern CPUs. The simulation results are presented in Figure 7.16. When an input power of -40 dBm is applied, the final output voltage V_{BOOST} passes the 1 V at around 3 seconds, the charge burst cycle is roughly 1 second. When an input power of -36 dBm is applied, V_{BOOST} passes the 1 V at around 1.2 seconds, the charge-burst cycle is roughly 0.3 seconds.

7.5.2 Design Verification over Process Variation

As discussed in the previous subsection, the full transient simulation is extremely long and thus, this brute-force approach is not feasible for the design verification over all technology corners. Hence, behaviour modelling of the RF front-end is necessary to accelerate the simulation time.

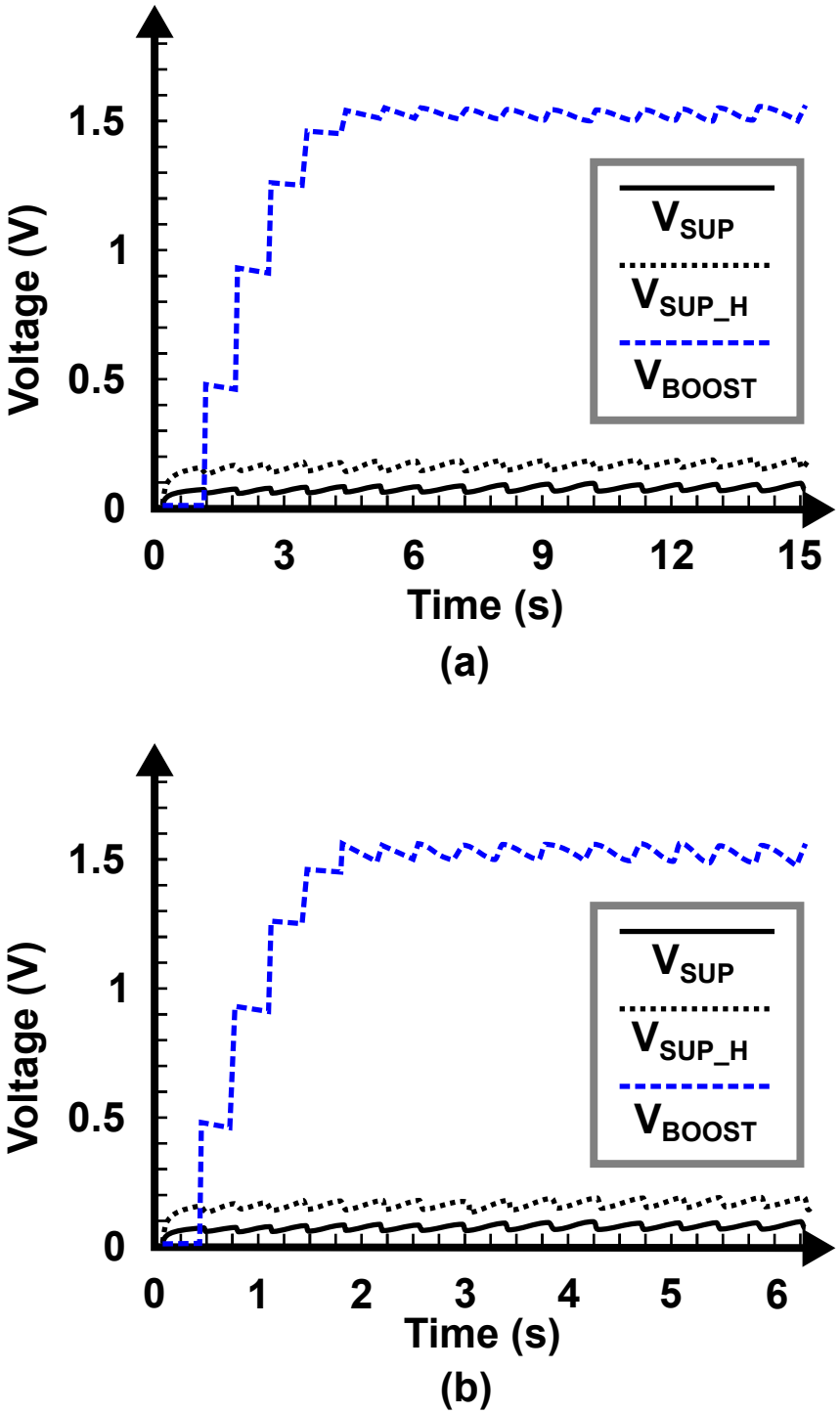


Figure 7.16. The simulated transient response of the overall charge-burst system under the input power of (a) −40 dBm (b) −36 dBm..

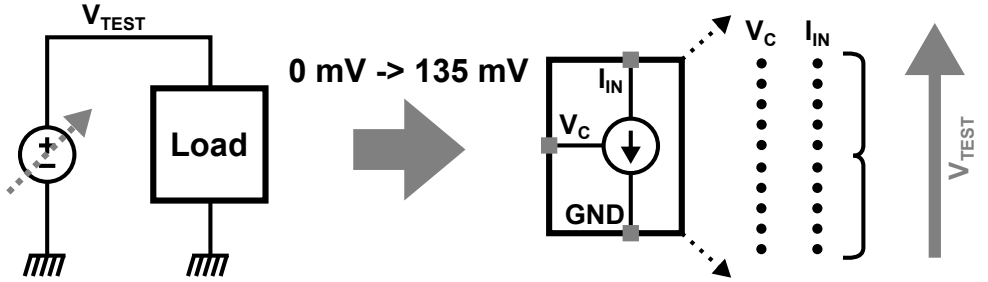


Figure 7.17. DC simulation to estimate the supply voltage and current consumption of the load.

Our approach relies on first characterizing the V/I properties of the load, which can then be used to derive the behavioural model of the rectifier that then can be used in the system-level verification. In our system, there are two rectifiers that needs to be modelled behaviourally, these are the main rectifier and the auxiliary rectifier. The load for the main rectifier is the step-up converter and the voltage detector, whereas the load for the auxiliary rectifier is the voltage level shifter. The current consumption of these loads depends on the supply voltage level. However, in the case of the step-up converter, its current consumption also depends the mode of operation.

In this work, we have combined the voltage detector and charge pump as the load which has different current consumption profiles depending on its mode of operation. The voltage detector asserts its output when the supply voltage passes 135 mV (typical corner) and turns on the charge pump. Because the charge pump consumes significantly more power than harvested in the low power domain, the supply voltage quickly falls, when it drops below 110 mV (typical corner), the voltage detector then de-asserts its output and turns off the charge pump. For V_{SUPH}, we simply assume that it is 200 mV (typical corner) higher than V_{SUP}. Because the burst period is significantly shorter than the charge period, the effect of burst current on rectifier's behavioural model was ignored. Thus, in this work, we are only characterising the OFF-mode load.

The supply voltage and current consumption relationship of the load under V_{SUP} (the voltage detector and the charge pump) and the load under V_{SUPH} (voltage level shift) can be characterised, using a DC simulation as shown in Figure 7.17. After the relationship between the supply voltage and current consumption is obtained, they can be loaded/filled into VCCSP (voltage controlled current source piecewise) component (analogLib) to form the behavioural model of the two loads. The next step is to simulate the full transistor level RF front-end together with the behavioural model

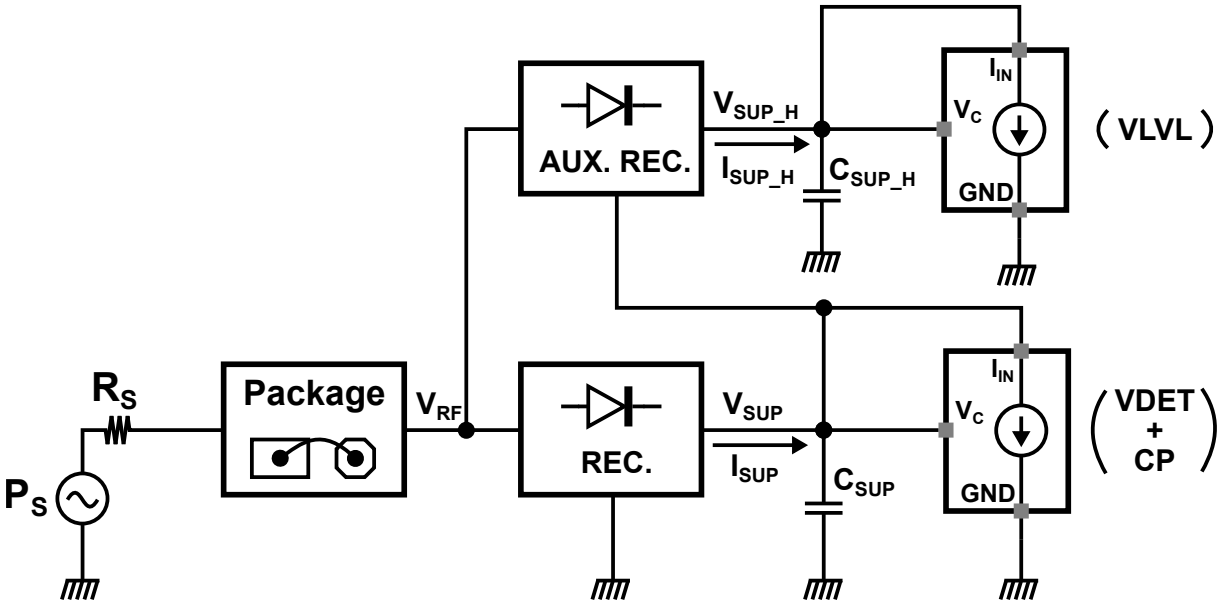


Figure 7.18. Simulation setup for deriving the behavioural model of the RF front-end rectifiers from behavioural models of the loads. Smaller values for C_{SUP} (1 nF) and C_{SUPH} (1 pF) are used to achieve fast settling time.

of the two loads. The purpose of this simulation is to derive the behavioural model of the RF front-end rectifiers (i.e. the main rectifier and the auxiliary rectifier.). This is the ultimate goal of the proposed modelling technique, because behavioural models of the front-end RF rectifier drastically reduce the simulation time. The simulation setup for the derivation of the RF front-end rectifier behavioural model is depicted in Figure 7.18. The C_{SUP} and C_{SUPH} used here are 1 nF and 1 pF, respectively. Relatively small capacitance values are used to achieve a faster settling. The simulation results are shown in Figure 7.19. It can be seen that V_{SUP} is roughly 200 mV low than V_{SUPH}, which validates the previous assumption about V_{SUPH} being 200 mV higher V_{SUP}.

After the values for V_{SUP}, I_{SUP}, V_{SUPH} and I_{SUPH} are obtained, we can load these into two separate VCCSP components to form the behavioural models for the main rectifier and the auxiliary rectifier. The behavioural models of the loads and front-end rectifiers have been developed over 16 simulation corners in addition to the typical corner, accounting for the process and temperature variations of N/P type MOSFETS, capacitors (resistors and BJTs are not used in the design) and temperature (-40 and 125 degrees). And the input power has been set to -35 dBm in all 16 corners. The overall transient response simulation of the charge-burst system has been conducted using previously derived behavioural model of the RF rectifier front-end together with

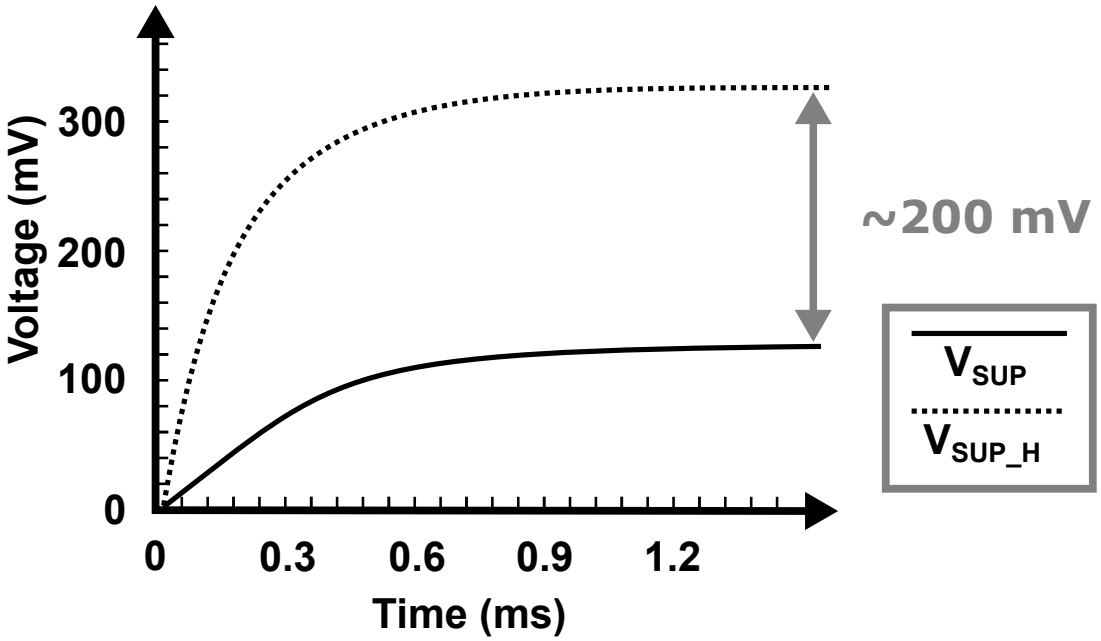


Figure 7.19. Simulation results for deriving the behavioural model of the RF front-end rectifiers from behavioural models of the loads. Smaller values for C_{SUP} (1 nF) and C_{SUPH} (1 pF) are used to achieve fast-settling.

transistor-level charge pump and control circuitry in matching simulation corners. It has been found that the system manages to start up and develop more than 1 V of final output in all corners, meaning the system is able to maintain an input power sensitivity of at least -35 dBm in the presence of process and temperature variation.

7.6 Conclusion

In this chapter, a charge-burst based energy harvester was demonstrated to develop more than 1 V at an input power of -40 dBm. The design achieves an astonishing result with the help of near-zero V_{TH} transistor, the proposed rectifier front-end sensitivity tuning scheme, the proposed charge-burst scheme, the leakage reduction switch for both the input and output of the charge pump and the proposed ultra-low-voltage charge pump. The performance metric of the stand-alone ultra-low-voltage charge pump and the overall energy harvester have been compared with prior-art designs in Table 7.1 and Table 7.2, respectively. It can be observed the proposed charge pump achieves a minimum operating input voltage as low as 85 mV, without the need for any external inductors while the proposed RF energy harvester

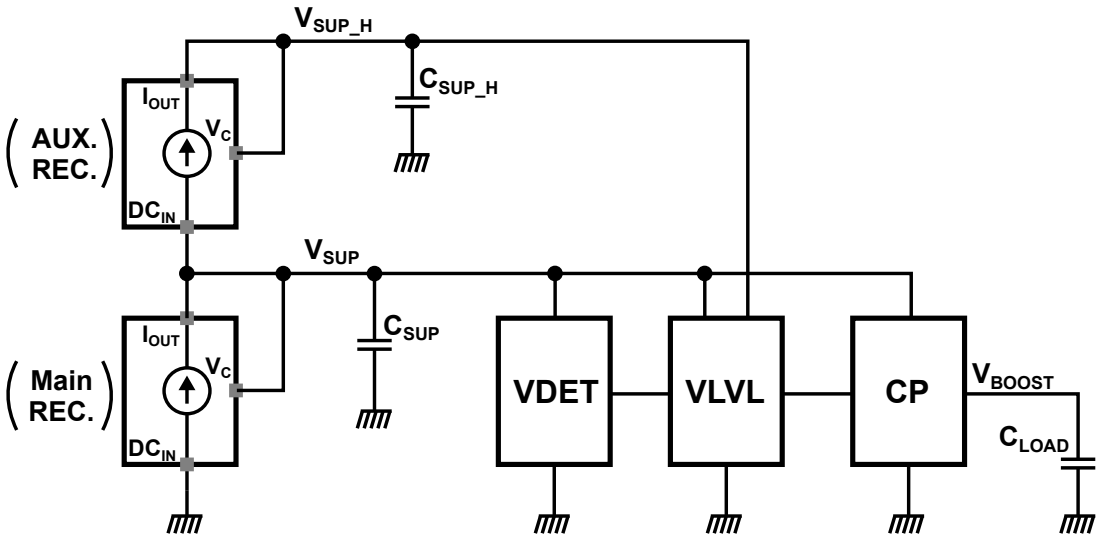


Figure 7.20. Simulation set-up for the overall charge-burst with behavioural models of the RF rectifiers and the transistor-level voltage detector, voltage level shift and the charge pump. The capacitor values used here are the standard values: 1 uF for C_{SUP}, 500 pF for C_{SUPH}, 500 pF for C_{LOAD}. VDET and VLVL stand for the voltage detector and voltage level shifter, respectively.

is superior in terms of input power sensitivity. The main contribution of this work is summarized as follows,

- Proposed an ultra-low-voltage charge pump that is capable of sub-100 mV operation
- Proposed using RF varactor to obtain a third degree of freedom in interface matching tuning
- Proposed an ultra-low-voltage voltage detector (around 100 mV) and charge-burst controller, which uses back-gate modulation to obtain a hysteresis in order of 10s of millivolts.
- Proposed a simulator-orientated approach to model the UHF rectifier, accounting for both the output loading and the RF interface mismatch.

The next chapter summarizes the whole thesis.

Table 7.1. Comparison the designed charge pump with prior-art design.

Design	Min. Vin	Vout	Ext. Comp.	Area (mm^2)	Pre-charge	Start-up
This work	85 mV	1.5 V@100 mV	No	0.32	No	No
(Ramadass et al., 2010)	35 mV	1.8 V@25 mV	3 inductors	1.7	1 V	N/A
(Carlson et al., 2010)	20 mV	0.9 V@50 mV	1 inductor	0.2	0.6 V	N/A
(Michelon et al., 2016)	200 mV	1.2 V@200 mV	1 inductor	0.09	N/A	N/A
(Goeppert et al., 2016)	70 mV	1.25 V@70 mV	1 inductor	0.6	N/A	Yes
(Guler et al., 2014)	85 mV	0.5 V@85 mV	N/A	1.8	N/A	Yes
(Fuketa et al., 2017)	100 mV	0.76 V@100 mV	N/A	2.4	N/A	Yes

Table 7.2. Comparison the designed UHF energy harvester with prior-art design.

Design	Tech.	Freq.	Sensitivity	Special Requirements
This work	130 nm	915 MHz	1.5 V@-40 dBm	Passive Booster
(Stoopman et al., 2014)	90 nm	868 MHz	1 V@-27 dBm	External MCU
(Michelon et al., 2016)	130 nm	915 MHz	1.2 V@-24 dBm	External inductor
(Oh et al., 2012)	130 nm	915 MHz	1 V@-32 dBm	Passive Booster
(Scorcioni et al., 2012)	130 nm	868 MHz	2 V@-17 dBm	Custom Antenna
(Abouzied et al., 2015)	180 nm	798 MHz	1 V@-27.3 dBm	Custom Antenna

Chapter 8

Conclusion

THIS chapter concludes the thesis and suggests future work.

This thesis can be divided into the following sections:

8.1 Part I: UHF Rectifier Design

Background: The design of highly sensitive UHF rectifier is very challenging. Because, as the input power and effectively input amplitude decreases, multiple trade-off for design emerges. Additionally, the non-linear nature of the rectifier during both steady-state and dynamic settling renders linear circuit theories irrelevant, making the design process less intuitive. This mandates the designer to come up with creative abstraction to gain insights into circuit performance and behaviour, avoiding converging into non-optimal designs.

Methodology: We start the design process with the sizing of the individual rectifier stages. A simplified procedure, which directly relates the sizing to the loading scenario, is proposed to significantly simplify the design process. From this, the number of stages can be easily determined from the desired output voltage. Finally, good matching needs to occur at the desired input power to achieve the excellent the overall system efficiency.

Simulation Results: With 1 MΩ resistor load, 1 V DC voltage is developed at the output of the rectifier at −27.6 dBm input power level. With proper adjustment of the source impedance, the peak PCE achieved with 1 MΩ, 100 kΩ and 10 kΩ, are 66%, 67% and 63%.

Original contribution: An intuitive UHF rectifier sizing scheme is proposed. Compared to exhaustive simulation approaches (Papotto et al., 2011; Hameed et al., 2015), the proposed sizing scheme leads to significantly less simulations.

Future work: This work has the potential to be further developed into a rectifier automatic sizing algorithm, which greatly accelerates the IP development process.

8.2 Part II: Reconfigurable threshold-compensated rectifiers

8.2.1 Optimizing the steady state performance of threshold compensated rectifiers

Background: In most threshold compensated rectifier designs, the threshold compensation voltage is proportional to the output voltage. Hence, threshold compensation performance and subsequently the conversion efficiency is tightly coupled with the output voltage of the rectifier. On the other hand, the conversion efficiency is also a weak of input amplitude.

Methodology: To maintain the output voltage across a single stage rectifier, in the low power mode, a 6-stage rectifier is employed, and its output DC voltage is regulated to 3 V. As input power increases, the input amplitude also increases. Hence, to compensate for the increased input amplitude, 6 6-stage rectifiers, effective 6 times the number of single-stage rectifiers in the low power mode, are configured in parallel to produce the final output voltage. In addition, a serially connected inductor was added in the low power mode to compensate for the increase in the reactive input impedance. Input power level is sensed by taking a tiny slice of the regulated current and passing it through a resistor. Then, the developed voltage can be used as an indication of the input power level.

Results: A peak PCE of 80% was achieved and a conversion efficiency of more than 60% can be achieved over 20 dB of input power range.

Original contribution: An efficient analog solution was proposed for UHF rectifier to achieve high power conversion efficiency over a wide input power range, intelligent power sensing and reconfiguration.

Future work: An even larger input power range can be experimented and more reconfiguration steps can be implemented to maintain even higher PCE over the same input power range.

8.2.2 Optimizing the dynamic settling performance of threshold compensated rectifiers

Background: Threshold compensated rectifier exhibits similar output dependency during dynamic settling. Specifically, the PCE of the threshold compensated rectifiers is only optimal during part of the settling process. For the rest of the settling process. the output voltage is either too high too low for the threshold compensation to be

effective. In addition, the real part of the input impedance increases as the output voltage settles, deviating significantly from the ideal matching point.

Methodology: To mitigate this issue, a reconfigurable rectifier was proposed to reconfigure itself from 4 single-stage rectifiers in parallel, to two 2-stage rectifiers in parallel, ultimately to one 4-stage rectifier, as the output of the rectifier settles. In addition to maintaining high PCE, the proposed reconfiguration scheme also compensates the rising real part of the input impedance, result in better matching over a much greater proportion of the settling period.

Results: At an input power of -24 dBm, the settling speed is demonstrated to be 1.74 times of that of the fixed 4-stage rectifier. The design has also been demonstrated to settle faster over a wide range of input power.

Original contribution: Exploited the output dependency of threshold compensation in the dynamic settling, proposed a reconfigurable rectifier settles significantly faster than its fixed counterpart.

Future work: More reconfiguration steps can be experimented to achieve even faster settling.

8.3 Part III: Power Management for UHF Energy Harvesting

Background: In a real UHF energy harvesting application scenario, the distance between the harvester and radiating source varies from time to time. As a result, the harvested power varies significantly from time to time. In other words, there are often times when the harvested power is more than the needed power and also times when the harvested power is insufficient. It is, therefore, useful to save the extra power and use it when the harvested power falls below the operational level.

Methodology: An excessive energy management unit (EEMU) was proposed to extract the excess energy and store it in the temporary storage capacitor. The EEMU consists of a negative feedback loop that regulates the output voltage of the rectifier by pulling current from it. The current will then be pumped onto a storage capacitor. When the harvested power is insufficient, the stored energy will be routed to power the system.

Results: With the EEMU and power routing, it has been demonstrated that the input power sensitivity can be potentially improved from -5 dBm to -30 dBm.

Original contribution: EEMU and Power routing unit were proposed to improve the responsiveness and cold start-up speed of the system.

Future work: Since the excessive energy is now stored for later use, it is now useful to achieve high conversion efficiency at all input power. The option of combining the PMU in this chapter with the high efficiency harvester proposed in chapter 4 is worth exploring.

8.4 Part IV: Energy Harvesting System

In this final section, we propose an ultra-sensitive harvester system which is able to develop more than 1 V with an input power of -40 dBm. This was made possible by having combining a RF harvester front-end with a secondary voltage booster.

Background and Methodology: In realm of UHF energy harvesting, developing a 1 V across a capacitive load at an input power -40 dBm is an unknown territory. To ultimately improve the input power sensitivity of the rectifier, charge burst technique needs to be employed. A secondary voltage booster can be used to boost the intermediate voltage developed by the front-end UHF rectifier.

Results: At input power of -40 dBm, the harvester develops an iconic 1.5 V across a capacitor load.

Original contribution: Achieving such a ground-breaking result requires circuit-level innovations in multiple aspects of the system and they are high-lighted as below,

- A varactor is employed in the passive booster to provide a third degree in tuning the RF interface.
- An ultra-low voltage and ultra-low power charge pump was designed to boost the intermediate voltage (around 100 mV) developed by the front-end rectifier.
- An ultra-low voltage and ultra-low power voltage detector and voltage comparator has been designed to control the charge-burst actions of the front-end rectifier and the charge pump.

Future work: As the system is particularly optimized for ultra-low input power, the system conversion efficiency will drop significantly when the input power increases. Hence, it is worth investigating approaches to reconfigure the system when the input power to maintain system efficiency.

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Biography

Menghan Sun received his B.Eng degree in Electrical Engineering from the University of Queensland, Brisbane, Australia in 2011 and M.Sc in Nano-electronic Engineering (majored in Analogue/RF IC Design) from Melbourne University, Melbourne, Australia in 2013.

Since September 2013, he was with Synochip Pty. Ltd., designing low-power analogue IC modules, including LDO, PLL and HF RFID tag chips.

In Dec 2014, he was awarded an Australian Postgraduate Award (APA) Scholarship to pursue his PhD under Dr Said Al-Sarawi and Prof. Derek Abbott, in the School of Electrical & Electronic Engineering. His area of research is in integrated solutions for UHF energy harvesting and power management.

Since Jun 2018, he has been with Silanna Semiconductor, working as Analog IC Designer.

Mr Sun has published a number of high-impact international journal and conference articles. He has a wide of range experience and expertise in the area of Analogue/RF IC Design.

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Scientifc Genealogy of Menghan Sun

"If I have seen further it is by standing on the shoulders of Giants."
Isaac Newton