O. Kavehei, A. Iqbal, Y. S. Kim, K. Eshraghian, S. F. Al-Sarawi and D. Abbott
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Proceedings of the Royal Society of London Series A-Mathematical Physical and Engineering Sciences, 2010; 466(2120):2175-2202

Originally Published at:
http://dx.doi.org/10.1098/rspa.2009.0553

The Fourth Element: Characteristics, Modelling, and Electromagnetic Theory of the Memristor

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In 2008, researchers at HP Labs published a paper in *Nature* reporting the realisation of a new basic circuit element that completes the missing link between charge and flux-linkage, which was postulated by Leon Chua in 1971. The HP memristor is based on a nanometer scale TiO_2 thin-film, containing a doped region and an undoped region. Further to proposed applications of memristors in artificial biological systems and nonvolatile RAM (NVRAM), they also enable reconfigurable nanoelectronics. Moreover, memristors provide new paradigms in application specific integrated circuits (ASICs) and field programmable gate arrays (FPGAs). A significant reduction in area with an unprecedented memory capacity and device density are the potential advantages of memristors for Integrated Circuits (ICs). This work reviews the memristor and provides mathematical and SPICE models for memristors. Insight into the memristor device is given via recalling the quasi-static expansion of Maxwell's equations. We also review Chua's arguments based on electromagnetic theory.

Keywords: Memristor, SPICE macro-model, Nonlinear circuit theory, Nonvolatile memory, Dynamic systems

1. Introduction

Based on the *International Technology Roadmap for Semiconductors* (ITRS) report [ITRS, 2007], it is predicted that by 2019, 16 nm half-pitch Dynamic Random Access Memory (DRAM) cells will provide a capacity around 46 GB/cm^2, assuming 100% area efficiency. Interestingly, memristors promise extremely high capacity more than 110 GB/cm^2 and 460 GB/cm^2 for 10 nm and 5 nm half-pitch devices, respectively [Williams, 2008, Lewis and Lee, 2009]. In contrast to DRAM memory, memristors provide nonvolatile operation as is the case for flash memories. Hence, such devices can continue the legacy of Moore's law for another decade. Furthermore, inclusion of molecular electronics and computing as an alternative to CMOS technologies in the recent ITRS report emphasises the significant challenges of device scaling [Jones, 2009]. Moreover, Swaroop et al. [1998] demonstrated that the complexity of a synapse, in an analog VLSI neural network implementation, is minimised by using a device called the *Programmable Metallization Cell* (PMC). This is an ionic programmable resistive device and a memristor can be employed to play the same role.

Research on memristor applications in various areas of circuit design, alternative materials and spintronic memristors, and especially memristor device/circuit modeling have appeared in the recent literature, (i) SPICE macro-modeling using linear and non-linear drift models [Chen and Wang, 2009, Zhang et al., 2009, Biolek et al., 2009b, Benderli and Wey, 2009, Kavehei et al., 2009, Wang et al., 2009a], (ii) Application of memristors in different circuit configurations and their dynamic behaviour [Li et al., 2009, Sun et al., 2009b, Wang et al., 2009b, Sun et al., 2009a], (iii) Application of memristor based dynamic systems to image encryption in Lin and Wang [2009], (iv) Fine resolution programmable resistor using a memristor in Shin et al. [2009], (v) Memristor-based op-amp circuit and filter characteristics of memristors by Yu et al. [2009] and Wang et al. [2009c], respectively, (vi) Memristor receiver (MRX) structure for ultra-wide band (UWB) wireless systems [Itoh and Chua, 2008, Witrisal, 2009], (vii) Memristive system I/O nonlinearity cancellation in Delgado [2009], (viii) The number of required memristors to compute a $f : \mathbb{R}^n \rightarrow \mathbb{R}^m$ function by Lehtonen and Laiho [2009], and its digital logic implementation using a memristor-based crossbar architecture in Raja and Mourad [2009], (ix) Different physical mechanisms to store information in memristors [Driscoll et al., 2009, Wang et al., 2009d], (x) Interesting fabricated nonvolatile memory using a *flexible memristor*, which is an inexpensive and low-power device solution is also recently reported [Gergel-Hackett et al., 2009], (xi) Using the *memductance* concept to develop an equivalent circuit diagram of a transmission-line has been carried out by Mallégol [2003, appendix 2].

There are still many problems associated with memristor device level. For instance, it is not clear that which leakage mechanisms are associated with the device. The *flexible memristor* is able to retain its nonvolatile characteristic for up to 14 days or, equivalently, up to 4000 flexes [Gergel-Hackett et al., 2009]. Thus, the nonvolatility feature eventually vanishes after a short period. Strukov and Williams [2009] also investigated this particular feature as a ratio of volatility to switching time.

One disadvantage of using memristors is switching speed. The volatility-to-switching speed ratio for memristor cells, in the HP cross-bar structure is around 10^3 [Strukov and Williams, 2009], which is much lower than the ratio for DRAM cells, 10^6 [ITRS, 2007], therefore, the switching speed of memristors is far behind DRAM. However, unlike DRAM, RRAM is non-volatile. In terms of yield, DRAM and RRAM are almost equal [Lewis and Lee, 2009]. Generally, endurance becomes very important once we note that the DRAM cells must be refreshed at least every 16 ms, which means at least 10^{10} write cycles in their life time [Lewis and Lee, 2009]. Unfortunately, memristors are far behind DRAM in terms of the endurance view point, but the HP team is confident that there is no functional limitation against improvement of memristor [Williams, 2008]. Finally, another advantage of RRAM is readability. Readability refers to the ability of a memory cell to report its state. This noise immunity in DRAM is weak because each DRAM cell stores a very small amount of charge particularly at nanometer dimensions, while in RRAM cells, e.g. memristors, it depends on the difference between the on and off state resistances [Lewis and Lee, 2009]. This difference was reported up to one order of magnitude [Williams, 2008].

It is interesting to note that there are devices with similar behaviour to a memristor, e.g. [Buot and Rajagopal, 1994, Beck et al., 2000, Krieger et al., 2001, Liu et al., 2006, Waser and Masakazu, 2007, Ignatiev et al., 2008, Tulina et al., 2008], but the HP scientists were the only group that found the link between their work and the missing memristor postulated by Chua. Moreover, it should be noted that physically realised memristors must meet the mathematical requirements of a memristor device or memristive systems that are discussed in Kang [1975] and Chua and Kang [1976]. For instance, the hysteresis

loop must have a double-valued bow-tie trajectory. However, for example in Krieger et al. [2001], the hysteresis loop shows more than two values for some applied voltage values. Beck et al. [2000] demonstrates one of the perfect examples of memristor devices. Kim et al. [2009a] recently introduced a multilevel one-time programmable (OTP) oxide diode for crossbar memories. They focused on a one-time programmable structure that basically utilises one diode and one resistor, 1D-1R, since obtaining a stable device for handling multiple programming and erasing processes is much more difficult than a one-time programmable device. In terms of functionality, OTP devices are very similar to memristive elements, but in terms of flexibility, memristors are able to handle multiple programming and erasing processes.

This paper focuses on the memristor device and reviews its device level properties. Although the memristor as a device is new, it was conceptually postulated by Chua [1971]. Chua predicted that a memristor could be realised as a purely dissipative device as a fourth fundamental circuit element. Thirty seven years later, Stan Williams and his group in the Information and Quantum Systems (IQS) Lab at HP realised the memristor in device form [Strukov et al., 2008].

In Section 2, we review the memristor and its characteristics as a nano-switch, which was realised by Hewlett-Packard (HP) [Strukov et al., 2008], and we review its properties based on the early mathematical models. We introduce a new model using a parameter we call the *resistor modulation index* (RMI). Due to the significance of ionic drift that plays the most important role in the memristive effect, this section is divided into two: (a) a linear, and (b) a nonlinear drift model. Section 3 presents a preliminary SPICE macro-model of the memristor and different types of circuit elements in combination with a proposed memristor macro-model. Section 4 describes an interpretation of the memristor based on electromagnetic theory by recalling Maxwell's equations. Finally, we summarise this review in Section 5.

2. Memristor Device Properties

Traditionally there are only three fundamental passive circuit elements: capacitors, resistors, and inductors, discovered in 1745, 1827, and 1831, respectively. However, one can set up five different mathematical relations between the four fundamental circuit variables: electric current i, voltage v, electric charge q, and magnetic flux φ. For *linear* elements, $f(v,i) = 0$, $f(v,q) = 0$ where $i = \frac{dq}{dt}$ ($q = Cv$), and $f(i,\varphi) = 0$ where $v = \frac{d\varphi}{dt}$ ($\varphi = Li$), indicate linear resistors, capacitors, and inductors, respectively.

In 1971, Leon Chua, proposed that there should be a fourth fundamental passive circuit element to set up a mathematical relationship between q and φ, which he named the *memristor* (a portmanteau of *memory* and *resistor*) [Chua, 1971]. Chua predicted that a class of memristors might be realisable in the form of a pure solid-state device without an internal power supply.

In 2008, Williams et al., at Hewlett Packard, announced the first fabricated memristor device [Strukov et al., 2008]. However, a resistor with memory is not a new thing. If taking the example of nonvolatile memory, it dates back to 1960 when Bernard Widrow introduced a new circuit element named the *memistor* [Widrow et al., 1960]. The reason for choosing the name of memistor is exactly the same as the memristor, a resistor with memory. The memistor has three terminals and its resistance is controlled by the time integral of a control current signal. This means that the resistance of the memistor is controlled by charge. Widrow devised the memistor as an electrolytic memory element to form a

basic structure for a neural circuit architecture called ADALINE (ADAptive LInear NEuron), which was introduced by him and his postgraduate student, Marcian Edward "Ted" Hoff [Widrow et al., 1960]. However, the memistor is not exactly what researchers were seeking at the nanoscale. It is just a charge-controlled three-terminal (transistor) device. In addition, a two-terminal nano-device can be fabricated without nanoscale alignment, which is an advantage over three-terminal nano-devices [Lehtonen and Laiho, 2009]. Furthermore, the electrochemical memistors could not meet the requirement for the emerging trend of solid-state integrated circuitry.

Thirty years later, Thakoor et al. [1990] introduced a solid-state thin-film tungsten-oxide-based, nonvolatile memory. The concept is almost similar to the HP memristors. Their solid-state memistor is electrically reprogrammable, it has variable resistance, and it is an analog synaptic memory connection that can be used in electrical neural networks. They claimed that the resistance of the device could be stabilised at any value, between 100 kΩ and 1 GΩ. This solid-state memistor has a thick, 60-80 nm, layer of silicon dioxide that achieves nonvolatility over a period of several months. This thick electron blocking layer, however, causes a considerable reduction in the applied electric field. As a consequence, they reported very high programming voltages ($\pm$ 25 to 30) and very long (minutes to hours) switching times.

In the 1960s, the very first report on the hysteresis behaviour of current-voltage curve was published by Simmons [1963], which is known as the *Simmons tunneling theory*. The Simmons theory generally characterises the tunneling current in a Metal-Insulator-Metal (MIM) system. A variable resistance with hysteresis was also published by Simmons and Verderber [1967]. They introduced a thin-film (20 to 300 nm) silicon dioxide doped with gold ions sandwiched between two 200 nm metal contacts. Thus overall the device is a MIM system, using aluminum metal contacts. Interestingly, their system demonstrates a sinh function behaviour as also recently reported in Yang et al. [2008] for the HP memristor. It is also reported that the switching from high- to low impedance takes about 100 ns. As their device is modelled as an energy storage element it cannot be a memristor, because memristors remember the total charge passing through the port and do not store charge [Oster, 1974].

The sinh resistance behaviour of memristors can be utilised to compensate the linearity of analog circuits. In Varghese and Gandhi [2009] a memristor based amplifier was proposed utilising the behaviour of a sinh resistor [Tavakoli and Sarpeshkar, 2005] as a memristor element. In Shin et al. [2009] such a structure was also introduced as an example without mentioning the sinh resistance behaviour of memristors. The idea in Tavakoli and Sarpeshkar [2005] is to characterise a sinh function type circuit that can be used to linearise a tanh function type circuit behaviour, e.g. CMOS differential amplifier. A theoretical analysis shows that a sinh function significantly reduces the third harmonic coefficient and as a consequence reduces nonlinearity of circuit.

Chua mathematically predicted that there is a solid-state device, which defines the missing relationship between four basic variables [Chua, 1971]. Recall that a resistor establishes a relation between voltage and current, a capacitor establishes a charge-voltage relation, and an inductor realises a current-flux relationship, as illustrated in Fig. 1. Notice that we are specifically discussing nonlinear circuit elements here.

Consequently, $\varphi = f_{\mathrm{M}}(q)$ or $q = g_{\mathrm{M}}(\varphi)$ defines a charge-controlled (flux-controlled) memristor. Then, $\frac{d\varphi}{dt} = \frac{df_{\mathrm{M}}(q)}{dq}\frac{dq}{dt}$ or $\frac{dq}{dt} = \frac{dg_{\mathrm{M}}(\varphi)}{d\varphi}\frac{d\varphi}{dt}$, which implies $v(t) = \frac{df_{\mathrm{M}}(q)}{dq}i(t)$ or $i(t) = \frac{dg_{\mathrm{M}}(\varphi)}{d\varphi}v(t)$. Note that, $M(q) = \frac{df_{\mathrm{M}}(q)}{dq}$ for a charge-controlled memristor and $W(\varphi) = \frac{dg_{\mathrm{M}}(\varphi)}{d\varphi}$ for a flux-controlled memristor, where $M(q)$ is the incremental memristance and

Figure 1. The four fundamental two-terminal circuit elements. There are six possible relationships between the four fundamental circuit variables, current (i), voltage (v), charge (q), and magnetic flux (φ). Out of these, five relationships are known comprising, $i = \frac{dq}{dt}$ and $v = \frac{d\varphi}{dt}$, and three circuit elements: resistor (R), capacitor (C), and inductor (L). Resistance is the rate of voltage change with current, inductance is the rate of flux change with current, capacitance is the rate of charge change with voltage. The only missing relationship is the rate of flux change with voltage (or vice-versa) that leads to the fourth element, a memristor. Adapted from Strukov et al. [2008].

$W(\varphi)$ is the incremental memductance where $M(q)$ is in the units of Ohms and the units of $W(\varphi)$ is in Siemens [Chua, 1971].

Memristance, $M(q)$, is the slope of the φ-q curve, which for a simple case, is a piecewise φ-q curve with two different slopes. Thus, there are two different values for $M(q)$, which is exactly what is needed in binary logic. For detailed information regarding typical φ-q curves, the reader is referred to Chua [1971].

It is also obvious that if $M(q) \geq 0$, then instantaneous power dissipated by a memristor, $p(i) = M(q)(i(t))^2$, is always positive so the memristor is a passive device. Thus the φ-q curve is a monotonically-increasing function. This feature is exactly what is observed in the HP memristor device [Strukov et al., 2008]. Some other properties of the memristor such as zero-crossing between current and voltage signals can be found in Chua [1971] and Chua and Kang [1976]. The most important feature of a memristor is its pinched hysteresis loop v-i characteristic [Chua and Kang, 1976]. A very simple consequence of this property and $M(q) \geq 0$ is that such a device is purely dissipative like a resistor.

Another important property of a memristor is its excitation frequency. It has been shown that the pinched hysteresis loop is shrunk by increasing the excitation frequency [Chua and Kang, 1976]. In fact, when the frequency increases toward infinity, the memristor acts as a linear resistor [Chua and Kang, 1976].

Interestingly enough, an attractive property of the HP memristor [Strukov et al., 2008], which is exclusively based on its fabrication process, can be deduced from the HP memristor simple mathematical model [Strukov et al., 2008] and is given by,

$$M(q) = R_{\mathrm{OFF}}\left(1 - \frac{R_{\mathrm{ON}}}{\beta}q(t)\right), \tag{2.1}$$

where β has the dimensions of magnetic flux $\varphi(t)$. Here, $\beta = \frac{D^2}{\mu_{\mathrm{D}}}$ in units of $\mathrm{sV} \equiv \mathrm{Wb}$, where μ_{D} is the average drift mobility in unit of $\mathrm{cm}^2/\mathrm{sV}$ and D is the film (titanium

dioxide, TiO_2) thickness. Note that R_{OFF} and R_{ON} are simply the 'on' and 'off' state resistances as indicated in Fig. 2. Also $q(t)$ defines the total charge passing through the memristor device in a time window, t - t_0. Notice that the memristor has an internal state [Chua and Kang, 1976]. Furthermore, as stated in Oster [1974], $q(t) = \int_{t_0}^{t} i(\tau)d\tau$, as the state variable in a charge-controlled memristor gives the charge passing through the device and does not behave as storage charge as in a capacitor as incorrectly reported in some works, e.g. Simmons and Verderber [1967]. This concept is very important from two points of view. First of all, a memristor is not an energy-storage element. Second, this shows that the memristor is not merely a nonlinear resistor, but is a nonlinear resistor with charge as a state variable [Oster, 1974].

Five years after Chua's paper on the memristor [Chua, 1971], he and his graduate student, Kang, published a paper defining a much broader class of systems, named *memristive systems*. From the memristive systems viewpoint a generalized definition of a memristor is $v(t) = R(w)i(t)$, where w defines the internal state of the system and $\frac{dw}{dt} = f(w,i)$ [Chua and Kang, 1976]. Based on this definition a memristor is a special case of a memristive system.

The HP memristor [Strukov et al., 2008] can be defined in terms of memristive systems. It exploits a very thin-film TiO_2 sandwiched between two platinum (Pt) contacts and one side of the TiO_2 is doped with oxygen vacancies, which are positively charged ions. Therefore, there is a TiO_2 junction where one side is doped and the other is undoped. Such a doping process results in two different resistances: one is a high resistance (undoped) and the other is a low resistance (doped). Hence, HP intentionally established a device that is illustrated in Fig. 2. The internal state variable, w, is also the variable length of the doped region. Roughly speaking, when $w \to 0$ we have nonconductive channel and when $w \to D$ we have conductive channel. The HP memristor switching mechanism is further discussed in Yang et al. [2008].

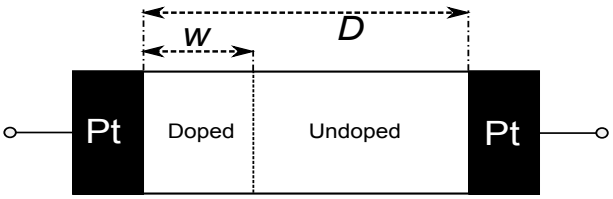

Figure 2. Schematic of HP memristor, where D is the device channel length and w is the length of doped region. The size of doped region is a function of the applied charge and is responsible for memristive effect as it changes the effective resistance of the device. Usually w is shown by its normalised counterpart, $x = w/D$. Adapted from Strukov et al. [2008].

(*a*) *Linear drift model*

The memristor's state equation is at the heart of the HP memristive system mechanism [Wang, 2008, Joglekar and Wolf, 2009]. Let us assume a uniform electric field across the device, thus there is a linear relationship between drift-diffusion velocity and the net electric field [Blanc and Staebler, 1971]. Therefore the state equation is,

$$\frac{1}{D}\frac{dw(t)}{dt} = \frac{R_{ON}}{\beta}i(t)\ . \tag{2.2}$$

Integrating Eq. 2.2 gives $\frac{w(t)}{D} = \frac{w(t_0)}{D} + \frac{R_{ON}}{\beta} q(t)$, where $w(t_0)$ is the initial length of w. Hence, the speed of drift under a uniform electric field across the device is given by $v_D = \frac{dw(t)}{dt}$. In a uniform field we have $D = v_D \times t$. In this case $Q_D = i \times t$ also defines the amount of required charge to move the boundary from $w(t_0)$, where $w \to 0$, to distance $w(t_D)$, where $w \to D$. Therefore, $Q_D = \frac{\beta}{R_{ON}}$, so

$$\frac{w(t)}{D} = \frac{w(t_0)}{D} + \frac{q(t)}{Q_D} \, . \tag{2.3}$$

If $x(t) = \frac{w(t)}{D}$ then

$$x(t) = x(t_0) + \frac{q(t)}{Q_D} \, , \tag{2.4}$$

where $\frac{q(t)}{Q_D}$ describes the amount of charge that is passed through the channel over the required charge for a conductive channel.

Using Strukov et al. [2008] we have,

$$v(t) = \left(R_{ON} \, \frac{w(t)}{D} + R_{OFF} \left(1 - \frac{w(t)}{D} \right) \right) i(t) \, . \tag{2.5}$$

By inserting $x(t) = \frac{w(t)}{D}$, Eq. 2.5 can be rewritten as

$$v(t) = \left(R_{ON} \, x(t) + R_{OFF} \left(1 - x(t) \right) \right) i(t) \, . \tag{2.6}$$

Now assume that $q(t_0) = 0$ then $w(t) = w(t_0) \neq 0$, and from Eq. 2.6,

$$M_0 = R_{ON} \left(x(t_0) + r \left(1 - x(t_0) \right) \right) \, , \tag{2.7}$$

where $r = \frac{R_{OFF}}{R_{ON}}$ and M_0 is the memristance value at t_0. Consequently, the following equation gives the memristance at time t,

$$M(q) = M_0 - \Delta R \left(\frac{q(t)}{Q_D} \right) \, , \tag{2.8}$$

where $\Delta R = R_{OFF} - R_{ON}$. When $R_{OFF} \gg R_{ON}$, $M_0 \approx R_{OFF}$ and Eq. 2.1 can be derived from Eq. 2.8.

Substituting Eq. 2.8 into $v(t) = M(q) i(t)$, when $i(t) = \frac{dq(t)}{dt}$, we have,

$$v(t) = \left(M_0 - \Delta R \left(\frac{q(t)}{Q_D} \right) \right) \frac{dq(t)}{dt} \, . \tag{2.9}$$

Recalling that $M(q) = \frac{d\varphi(q)}{dq}$, the solution is

$$q(t) = \frac{Q_D M_0}{\Delta R} \left(1 \pm \sqrt{1 - \frac{2\Delta R}{Q_D M_0^2} \varphi(t)} \right) \, . \tag{2.10}$$

Using $\Delta R \approx M_0 \approx R_{\rm OFF}$, Eq. 2.10 becomes,

$$q(t) = Q_D \left(1 - \sqrt{1 - \frac{2}{Q_D R_{\rm OFF}} \varphi(t)} \right) . \tag{2.11}$$

Consequently, using Eq. 2.4 if $Q_D = \frac{D^2}{\mu_D R_{\rm ON}}$, so the internal state of the memristor is

$$x(t) = 1 - \left(\sqrt{1 - \frac{2\mu_D}{rD^2} \varphi(t)} \right) . \tag{2.12}$$

The current-voltage relationship in this case is,

$$i(t) = \frac{v(t)}{R_{\rm OFF} \left(\sqrt{1 - \frac{2\mu_D}{rD^2} \varphi(t)} \right)} . \tag{2.13}$$

In Eq. 2.13, the inverse square relationship between memristance and TiO_2 thickness, D, shows that for smaller values of D, the memristance shows improved characteristics, and because of this reason the memristor imposes a small value of D.

In Eqs. 2.10-2.13, the only term that significantly increases the role of $\varphi(t)$ is lower $Q_{\rm D}$. This shows that at the micrometer scale $\frac{1}{R_{\rm OFF} Q_{\rm D}} = \frac{1}{r\beta} = \frac{\mu_{\rm D}}{rD^2}$ is negligible and the relationship between current and voltage reduces to a resistor equation.

Substituting $\beta = \frac{D^2}{\mu_D}$ that has the same units as magnetic flux into Eq. 2.13, and considering $c(t) = \frac{\varphi(t)}{\beta} = \frac{\mu_D \varphi(t)}{D^2}$ as a normalised variable, we obtain

$$i(t) = \frac{v(t)}{R_{\rm OFF} \left(\sqrt{1 - \frac{2}{r} c(t)} \right)} , \tag{2.14}$$

where $\sqrt{1 - \frac{2}{r} c(t)}$ is what we call the *resistance modulation index*, (RMI) [Kavehei et al., 2009].

Due to the extremely uncertain nature of nanotechnologies, a variability-aware modeling approach should be always considered. Two well-know solutions to analyse a memristive system were investigated in Chen and Wang [2009], 1) Monte-Carlo simulation for evaluating (almost) complete statistical behaviour of device, and 2) Corner analysis. Considering the trade-off between time-complexity and accuracy between these two approach as shows the importance of using a simple and reasonably accurate model, because finding the real corners is highly dependent on the model accuracy. The resistance modulation index, RMI, could be one of the device parameters in the model extraction phase, so it would help to provide a simple model with fewer parameters.

Joglekar and Wolf [2009] clarified the behaviour of two memristors in series. As shown in Fig. 3, they labeled the polarity of a memristor by $\eta = \pm 1$, where $\eta = +1$ signifies that $w(t)$ increases with positive voltage or, in other words, the doped region in memristor is expanding. If the doped region, $w(t)$, is shrinking with positive voltage, then $\eta = -1$. In other words, reversing the voltage source terminals implies memristor polarity switching. In Fig. 3 (a), the doped regions are simultaneously shrunk so the overall memristive effect is retained. In Fig. 3 (b), however, the overall memristive effect is suppressed [Joglekar and Wolf, 2009].

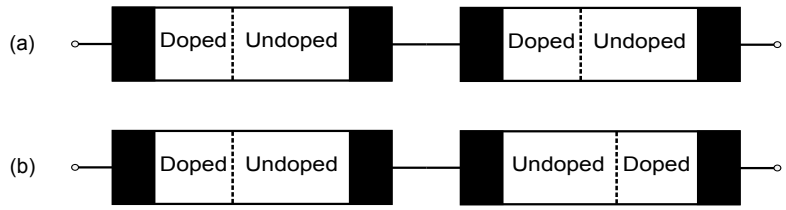

Figure 3. Two memristors in series, (a) With the same polarity, both $\eta = -1$ or both $\eta = +1$. (b) With opposite polarities, $\eta = -1$ and $\eta = +1$. Where $\eta = +1$ signifies that $w(t)$ increases with positive voltage or, in other words, the doped region in memristor is expanding and $\eta = -1$ indicates that the doped region is shrinking with applied positive voltage across the terminals. Adapted from Joglekar and Wolf [2009].

Using the memristor polarity effect and Eq. 2.2, we thus obtain

$$\frac{1}{D}\frac{dw(t)}{dt} = \eta \frac{R_{\rm ON}}{\beta} i(t) \; . \tag{2.15}$$

Then with similar approach we have

$$i(t) = \frac{v(t)}{R_{\rm OFF}\left(\sqrt{1 - \eta \frac{2}{r} c(t)}\right)} \; . \tag{2.16}$$

There is also no phase shift between current and voltage signals, which implies that the hysteresis loop always crosses the origin as demonstrated in Fig. 4. For further investigation, if a voltage, $v(t) = v_0 \sin(\omega t)$, is applied across the device, the magnetic flux would be $\varphi(t) = -\frac{v_0}{\omega}\cos(\omega t)$. The inverse relation between flux and frequency shows that at very high frequencies there is only a linear resistor.

Fig. 4 demonstrates Eq. 2.16 in MATLAB for five different frequencies, where $\omega_0 = \frac{2\pi v_0}{\beta}$, using the Strukov et al. [2008] parameter values, $D = 10$ nm, $\mu_D = 10^{-10}$ cm^2 s^{-1} V^{-1}, $R_{\rm ON} = 100\ \Omega$, $R_{\rm OFF} = 16$ kΩ, $v_0 = 1$ V, and $\eta = -1$. The *resistance modulation index*, RMI $= \sqrt{1 - \eta \frac{2}{r} c(t)}$ simulation with the same parameter values is shown in Fig. 5.

Using different parameters causes a large difference in the hysteresis and memristor characteristics. In Witrisal [2009], a new solution for ultra-wideband signals using memristor devices was introduced. Applying the parameter values given in Witrisal [2009] results in a significant difference in the value of ω_0. Substituting parameter values given in the paper gives $\omega_0 \approx 4$ GHz instead of $\omega_0 \approx 50$ kHz, using to $t_0 \approx 0.1$ ms and the parameter values from Strukov et al. [2008]. The new parameter values are $D = 3$ nm, $\mu_D = 3 \times 10^{-8}$ m^2 s^{-1} V^{-1}, $R_{\rm ON} = 100\ \Omega$, $R_{\rm OFF} = 10$ kΩ, and $v_0 = 0.2$ V. Using these parameters shows that even though the highest and lowest memristance ratio in the last case, Fig. 4, is around 2, here the ratio is approximately equal to 120.

(*b*) *Nonlinear drift model*

The electrical behaviour of the memristor is directly related to the shift in the boundary between doped and undoped regions, and the effectively variable total resistance of the device when an electrical field is applied. Basically, a few volts supply voltage across a very thin-film, e.g. 10 nm, causing a large electric field. For instance, it could be more than

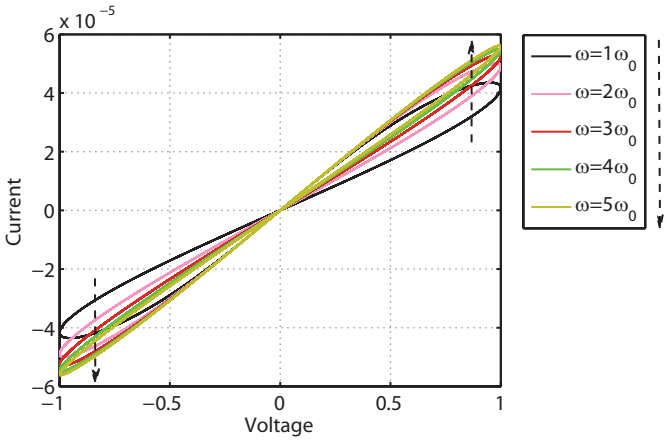

Figure 4. The hysteresis of a memristor based on Eq. 2.16. This verifies the hysteresis shrinks at higher frequencies. It also shows that the effective resistance is changing, so there is a varying memristance with a monotonically-increasing q-φ curve.

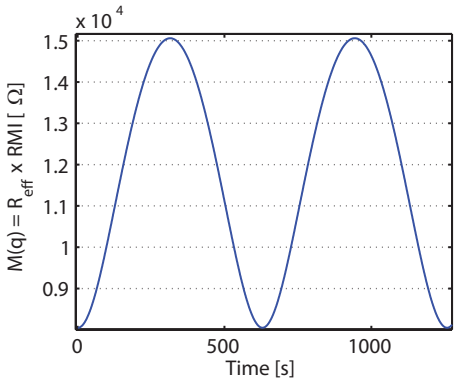

Figure 5. The hysteresis characteristics of the memristor. It shows that the memristance value is varying from a very low to a very high resistance. It is clear that these values depend on the parameter values, such as R_{on} and R_{off}.

10^6 V/cm, which results in a fast and significant reduction in energy barrier [Blanc and Staebler, 1971]. Therefore, it is reasonable to expect a high nonlinearity in ionic drift-diffusion [Waser et al., 2009].

One significant problem with the linear drift assumption is the boundaries. The linear drift model, Eq. 2.2, suffers from problematic boundary effects. Basically, at the nanoscale, a few volts causes a large electric field that leads to a significant nonlinearity in ionic transport [Strukov et al., 2008]. A few attempts have been carried out so far to consider this nonlinearity in the state equation [Strukov et al., 2008, Strukov and Williams, 2009, Biolek et al., 2009b, Benderli and Wey, 2009]. All of them proposed a simple *window function*, $F(\xi)$, which is multiplied by the right-hand side of Eq. 2.2. In general, ξ could be a variable vector, e.g. $\xi = (w, i)$ where w and i are the memristor's state variable and current, respectively.

In general, the window function can be multiplied by the right-hand side of the state variable equation, Eq. 2.2,

$$\frac{dx(t)}{dt} = \eta \frac{R_{\rm ON}}{\beta} i(t) F(x(t), p) \ , \tag{2.17}$$

where $x(t) = w(t)/D$ is the normalised form of the state variable. The window function makes a large difference between the model with linear and nonlinear drift assumptions at the boundaries. Fig. 6 shows such a condition considering a nonlinear drift assumption at the critical, or boundary, states. In other words, when a linear drift model is used, simulations should consider the boundaries and all constraints on initial current, initial voltage, maximum and minimum w, and etc. These constraints cause a large difference in output between linear and nonlinear drift assumptions. For example, it is impossible to achieve such a realistic curve, as in Fig. 6, using the linear drift modeling approach.

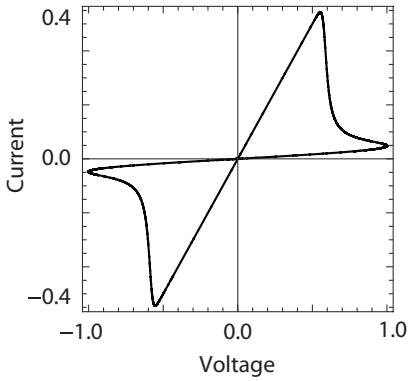

Figure 6. The hysteresis characteristics using the nonlinear drift assumption. This hysteresis shows a highly nonlinear relationship between current and voltage at the boundaries. To model this nonlinearity, there is a need for an additional term on the right hand side of the memristor's state equation, called a *window function*.

In Strukov et al. [2008], the window function is a function of the state variable and it is defined as $F(w) = w(1-w)/D^2$. The boundary conditions in this case are $F(0) = 0$ and $F(D) = \frac{1-D}{D} \approx 0$. It meets the essential boundary condition $F(\xi \to \text{boundaries}) = 0$, except there is a slight difference when $w \to D$. The problem of this boundary assumption is when a memristor is driven to the terminal states, $w \to 0$ and $w \to D$, then $\frac{dw}{dt} \to 0$, so no external field can change the memristor state [Biolek et al., 2009b]. This is a fundamental problem of the window function. The second problem of the window function is it assumes that the memristor remembers the amount of charge that passed through the device. Basically, this is a direct result of the state equation, Eq. 2.2, [Biolek et al., 2009b]. However, it seems that the device remembers the position of boundary between the two regions, and not the amount of charge.

In Benderli and Wey [2009], another window function has been proposed that is slightly different from that in Strukov et al. [2008]. This window function, $F(w) = w(D-w)/D^2$, approaches zero when $w \to 0$ and when $w \to D$ then $F(w) \to 0$. Therefore, this window function meets both the boundary conditions. In fact, the second window function is imitates the first function when we consider $x = w/D$ instead of w. In addition, there is another problem associated with these two window functions, namely, the modeling of approximate linear ionic drift when $0 < w < D$. Both of the window functions approximate nonlinear behaviour when the memristor is not in its terminal states, $w = 0$ or $w = D$. This problem is

addressed in Joglekar and Wolf [2009] where they propose an interesting window function to address the nonlinear and approximately linear ionic drift behaviour at the boundaries and when $0 < w < D$, respectively. Nonlinearity (or linearity) of their function can be controlled with a second parameter, which we call the *control parameter*, p. Their window function is $F(x) = 1 - (2x-1)^{2p}$, where $x = w/D$ and p is a positive integer. Fig. 7 (a) demonstrates the function behaviour for different $2 \leq p \leq 10$ values. This model considers a simple boundary condition, $F(0) = F(1) = 0$. As demonstrated, when $p \geq 4$, the state variable equation is an approximation of the linear drift assumption, $F(0 < x < 1) \approx 1$.

The most important problem associated with this model is revealed at the boundaries. Based on this model, when a memristor is at the terminal states, no external stimulus can change its state. Biolek et al. [2009b] tackles this problem with a new window function that depends on x, p, and memristor current, i. Basically, x and p are playing the same role in their model and the only new idea is using current as an extra parameter. The window function is, $F(x) = 1 - (x - \text{sgn}(-i))^{2p}$, where i is memristor current and $\text{sgn}(i) = 1$ when $i \geq 0$, and $\text{sgn}(i) = 0$ when $i < 0$. As a matter of fact, when the current is positive, the doped region length, w, is expanding. Fig. 7 (b) illustrates the window function behaviour.

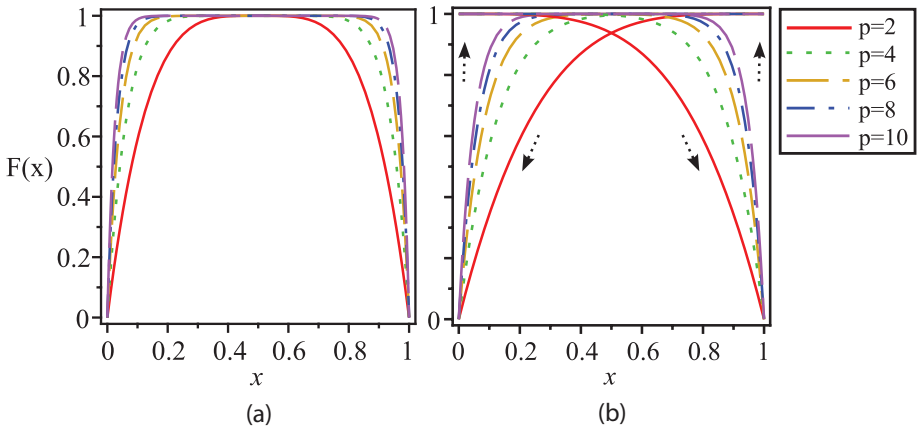

Figure 7. Non-linear window functions, (a) $F(x) = 1 - (2x-1)^{2p}$, (b) $F(x) = 1 - (x - \text{sgn}(-i))^{2p}$. There are around four window functions in the literature but these two are meet the boundary conditions.

All window functions suffer from a serious problem. They are only dependent on the state variable, x, which implies that the memristor remembers the entire charge that is passing through it. Moreover, based on the general definition of the time-invariant memristor's state equation and current-voltage relation, $\dot{x} = f(x,i)$ or $\dot{x} = g(x,v)$, f and g must be *continuous* n-dimensional vector functions [Kang, 1975, chap. 2]. However, the last window function, $F(x) = 1 - (x - \text{sgn}(-i))^{2p}$, does not provide the continuity condition at the boundaries, $x \to 0$ or $x \to 1$. Biolek et al. [2009b] did not use the window function in their recent publication [Biolek et al., 2009a].

In Strukov and Williams [2009] the overall drift velocity is identified with one linear equation and one highly nonlinear equation, $\upsilon = \mu E$, when $E << E_0$ and $\upsilon = \mu E_0 \exp(\frac{E}{E_0})$, for $E \sim E_0$, where υ is the average drift velocity, E is an applied electric field, μ is the mobility, and E_0 is the characteristic field for a particular mobile ion. The value of E_0 is typically about 1 MV/cm at room temperature [Strukov and Williams, 2009]. This equa-

tion shows that a very high electric field is needed for exponential ion transport. They also showed that the high electric field is lower than the critical field for dielectric breakdown of the oxide. Reviewing the available window functions indicates that there is a need for an appropriate model that can define memristor states for strongly nonlinear behavior where, $E \sim E_0$.

In addition to the weakness of nonlinear modeling in the original HP model, there are some other drawbacks that show the connection between physics and electronic behaviour was not well established. Moreover, the currently available electronic models for memristors followed the exact pathway of the HP modeling, which is mostly due to the fact that the underlying physical conduction mechanism is not fully clear yet [Kim et al., 2009b]. One weakness is that the HP model does not deliver any insight about capacitive effects, which are naturally associated with memristors. These capacitive effects will later be explained in terms of a memcapacitive effect in a class of circuit elements with memory. In Kim et al. [2009b] the memristor behaviour was realised using infinite number of crystalline magnetite (Fe_3O_4) nanoparticles. The device behaviour combines both memristive (time-varying resistance) and memcapacitive (time-varying capacitance) effects, which deliver a better model for the nonlinear properties. Their model description for current-voltage relationship is given as,

$$i(t) = \frac{v(t)}{\sqrt{R^2(x,t) + \frac{1}{i^2(t)}\left(\frac{q(t)}{C(x,t)}\right)^2}}\,, \tag{2.18}$$

where $R(x,t)$ and $C(x,t)$ are the time-varying resistance and capacitance effects, respectively. The time-dependent capacitor is a function of the state variable, $x(t) = w(t)/D$ and $\Delta C(t)$, where $\Delta C(t)$ is defined as the additional capacitance caused by changing the value of capacitance [Kim et al., 2009b], $C(x,t) = \frac{C_{\rm ON} - \Delta C(t)}{1-x(t)}$, where $C_{\rm ON}$ is the capacitance at $x = 0$. The state variable is also given by,

$$x(t) = \frac{1}{\beta}\left(R_{\rm ON} q(t) + \frac{\int_{t_0}^{t} q(\tau)\, d\tau}{C_{\rm ON} - \Delta C(t)}\right). \tag{2.19}$$

Kim et al. [2009b] also investigated the impact of temperature variation on their Fe_3O_4 nanoparticle memristor assemblies of D equal to 9, 12, and 15 nm. It was reported that the change in electrical resistivity (specific electrical resistance), ρ_r, as an explicit function of temperature can be defined by, $\log\rho_r = 1/\sqrt{T}$, which means there is a significantly increasing behaviour as temperature decreases. As a consequence, for example, there is no hysteresis loop signature at room temperature, $T = 295$ K, ($D = 12$ nm) while at $T = 210$ K it shows a nice bow-tie trajectory. As they claimed, the first room temperature reversible switching behaviour was observed in their nanoparticle memristive system [Kim et al., 2009b].

It is worth noting that there are also two other elements with memory named the *memcapacitor* (Memcapacitive, MC, Systems) and *meminductor* (Meminductive, MI, Systems). Di Ventra et al. [2009] postulated that these two elements also could be someday realised in device form. The main difference between these three elements, the memristor, memcapacitor, and meminductor is that, the memristor is not a lossless memory device and dissipates energy as heat. However, at least in theory, the memcapacitor and meminductor are lossless devices because they do not have resistance. Di Ventra et al. [2009] also investigated some

examples of using different nanoparticle-based thin-film materials. Memristors (Memresistive, MR, Systems) are identified by a hysteresis current-voltage characteristic, whereas MC and MI systems introduce Lissajous curves for charge-voltage and flux-current, respectively. Similar to memristors, there are two types of these elements, therefore, the three circuit elements with memory (mem-systems/devices) can be summarised as follows,

Memristors (MR Systems): A memristor is an one-port element whose instantaneous electric charge and flux-linkage, denoted by $q_{\rm mr}$ and $\varphi_{\rm mr}$, respectively, satisfy the relation $F_{\rm mr}(q_{\rm mr},\varphi_{\rm mr})=0$. It has been proven that these devices are passive elements [Strukov et al., 2008]. As discussed, they cannot store energy, so $v_{\rm mr}(t)=0$ whenever $i_{\rm mr}(t)=0$ and there is a pinched hysteresis loop between current and voltage. Thus, charge-flux curve is a monotonically-increasing function. A memristor acts as a linear resistor when frequency goes toward infinity and as a nonlinear resistor at low frequencies. Due to the nonlinear resistance effect, $\frac{dv_{\rm mr}}{dt}=R(t)\frac{di_{\rm mr}}{dt}+i_{\rm mr}(t)\frac{dR}{dt}$ should be utilised instead of $\frac{dv_{\rm mr}}{dt}=R(t)\frac{di_{\rm mr}}{dt}$. There are two types of control process,

I. nth order current-controlled MR systems †, $q_{\rm mr}=\int i_{\rm mr}(\tau)\,d\tau$,

- $v_{\rm mr}(t)=R(x,i_{\rm mr},t)i_{\rm mr}(t)$
- $\dot{x}=f_{\rm icmr}(x,i_{\rm mr},t)$

II. nth order voltage-controlled MR systems, $\varphi_{\rm mr}=\int v_{\rm mr}(\tau)\,d\tau$,

- $i_{\rm mr}(t)=R^{-1}(x,v_{\rm mr},t)v_{\rm mr}(t)$
- $\dot{x}=f_{\rm vcmr}(x,v_{\rm mr},t)$.

Memcapacitors (MC Systems): A memcapacitor is an one-port element whose instantaneous flux-linkage and time-integral of electric charge, denoted by $\varphi_{\rm mc}$ and $\sigma_{\rm mc}$, respectively, satisfy the relation $F_{\rm mc}(\varphi_{\rm mc},\sigma_{\rm mc})=0$. The total added/removed energy to/from a voltage-controlled MC system, $U_{\rm mc}=\int v_{\rm mc}(\tau)\,i_{\rm mc}(\tau)\,d\tau$, is equal to the linear summation of areas between $q_{\rm mc}$-$v_{\rm mc}$ curve in the first and third quadrants with opposite signs. Due to the nonlinear capacitance effect, $\frac{dq_{\rm mc}}{dt}=i_{\rm mc}(t)=C(t)\frac{dv_{\rm mc}}{dt}+v_{\rm mc}(t)\frac{dC}{dt}$ should be utilised instead of $\frac{dq_{\rm mc}}{dt}=C(t)\frac{dv_{\rm mc}}{dt}$, so $U_{\rm mc}=\int v_{\rm mc}C\,dv_{\rm mc}+\int v_{\rm mc}^2\,dC$. In principle a memcapacitor can be a passive, an active, and even a dissipative‡ element [Di Ventra et al., 2009]. If $v_{\rm mc}(t)=V_{\rm mc0}\cos(2\pi\omega t)$ and capacitance is varying between two constant values, $C_{\rm ON}$ and $C_{\rm OFF}$, then the memcapacitor is a passive element. It is also important to note that, assuming zero charged initial state for a passive memcapacitor, the amount of removed energy cannot exceed the amount of previously added energy [Di Ventra et al., 2009]. A memcapacitor acts as a linear capacitor when frequency tend to infinity and as a nonlinear capacitor at low frequencies. There are two types of control process,

I. nth order voltage-controlled MC systems, $\varphi_{\rm mc}=\int v_{\rm mc}(\tau)\,d\tau$,

- $q_{\rm mc}(t)=C(x,v_{\rm mc},t)v_{\rm mc}(t)$
- $\dot{x}=f_{\rm vcmc}(x,v_{\rm mc},t)$

† Current- (and voltage-) controlled is a better definition for memristors because they do not store any charge [Oster, 1974]. In Di Ventra et al. [2009] it is specified as current- (and voltage-) controlled instead of charge- (and flux-) controlled in Chua [1971].

‡ Adding energy to system.

II. *n*th order charge-controlled MC systems, $\sigma_{\rm mc} = \int q_{\rm mc}(\tau)\,d\tau = \iint i_{\rm mc}(\tau)\,d\tau$,

- $v_{\rm mc}(t) = C^{-1}(x, q_{\rm mc}, t)q_{\rm mc}(t)$
- $\dot{x} = f_{\rm qcmc}(x, q_{\rm mc}, t)$.

Meminductors (ML Systems): A meminductor is a one-port element whose instantaneous electric charge and time-integral of flux-linkage, denoted by $q_{\rm ml}$ and $\rho_{\rm ml}$, respectively, satisfy the relation $F_{\rm ml}(\rho_{\rm ml}, q_{\rm ml}) = 0$. In the total stored energy equation in a ML system, $U_{\rm ml} = \int v_{\rm ml}(\tau)\, i_{\rm ml}(\tau)\,d\tau$, the nonlinear inductive effect, $\frac{d\varphi_{\rm ml}}{dt} = v_{\rm ml}(t) = L(t)\frac{di_{\rm ml}}{dt} + i_{\rm ml}(t)\frac{dL}{dt}$ should be taken into account. Thus, $U_{\rm ml} = \int i_{\rm ml} L\, di_{\rm ml} + \int i_{\rm ml}^2\, dL$. Similar to MC systems, in principle a ML system can be a passive, an active, and even a dissipative element and using the same approach, under some assumptions they behave like passive elements [Di Ventra et al., 2009]. There are two types of control process,

I. *n*th order current-controlled ML systems, $q_{\rm ml} = \int i_{\rm ml}(\tau)\,d\tau$,

- $\varphi_{\rm ml}(t) = L(x, i_{\rm ml}, t)i_{\rm ml}(t)$
- $\dot{x} = f_{\rm icml}(x, i_{\rm ml}, t)$

II. *n*th order flux-controlled ML systems, $\rho_{\rm ml} = \int \varphi_{\rm ml}(\tau)\,d\tau = \iint v_{\rm ml}(\tau)\,d\tau$,

- $i_{\rm ml}(t) = L^{-1}(x, \varphi_{\rm ml}, t)\varphi_{\rm ml}(t)$
- $\dot{x} = f_{\rm fcml}(x, \varphi_{\rm ml}, t)$.

Biolek et al. [2009a] introduced a generic SPICE model for mem-devices. Their memristor model was discussed before in this section. Unfortunately, there are no simulation results available in Biolek et al. [2009a] for MC and ML systems.

It is worth noting that there is no equivalent mechanical element for the memristor. In Chen et al. [2009] a new mechanical suspension component, named a *J-damper*, has been studied. This new mechanical component has been introduced and tested in Formula One Racing, delivering significant performance gains in handling and grip [Chen et al., 2009]. In that paper, the authors attempt to show that the *J-damper*, which was invented and used by the McLaren team, is in fact an *inerter* [Smith, 2002]. The *inerter* is a one-port mechanical device where the equal and opposite applied force at the terminals is proportional to the relative acceleration between them [Smith, 2002]. Despite the fact that the *missing mechanical circuit element* has been chosen because of a "spy scandal" in the 2007 Formula One race [Formula1, 2007], it may be possible that a "real" missing mechanical equivalent to a memristor may someday be found, as its mechanical model is described by Oster [1973] and Oster [1974].

3. SPICE Macro-Model of memristor

Basically, there are three different ways available to model the electrical characteristics of the memristors. SPICE macro-models, hardware description language (HDL), and C programming. The first, SPICE macro-models, approach is more appropriate since it is more readable for most of the readers and available in all SPICE versions. There is also another reason for choosing SPICE modeling approach. Regardless of common convergence problems in SPICE modeling, we believe it is more appropriate way to describe real device operation. Moreover, using the model as a sub-circuit can highly guarantee a reasonably high flexibility and scalability features.

A memristor can be realised by connecting an appropriate nonlinear resistor, inductor, or capacitor across port 2 of an M-R mutator, an M-L mutator, or an M-C mutator, respectively † [Chua, 1971]. These mutators are nonlinear circuit elements that may be described by a SPICE macro-model (i.e. an analog behavioural model of SPICE). The macro circuit model realisation of a type-1 M-R mutator based on the first realisation of the memristor [Chua, 1971] is shown in Fig. 8.

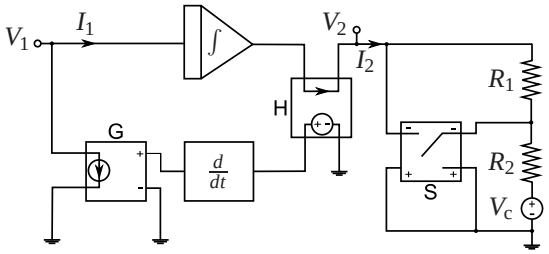

Figure 8. The SPICE macro-model of memristor. Here G, H and S are a Voltage-Controlled Current Source (VCCS), a Current-Controlled Voltage Source (CCVS), and a Switch ($V_{ON} = -1.9$ V and $V_{OFF} = -2$ V), respectively. $R_1 = R_2 = 1$ kΩ and $V_c = -2$ V. The M-R mutator consists of an integrator, a Current-Controlled Voltage Source (CCVS) "H", a differentiator and a Voltage-Controlled Current Source (VCCS) "G". The nonlinear resistor is also realised with resistors R_1, R_2, and a switch. Therefore, the branch resistance is 1 kΩ for $V < 2$ Volt and 2 kΩ for $V \geq 2$ Volt.

In this model the M-R mutator consists of an integrator, a Current-Controlled Voltage Source (CCVS) "H", a differentiator and a Voltage-Controlled Current Source (VCCS) "G". The nonlinear resistor is also realised with resistors R_1, R_2, and a switch. Therefore, the branch resistance is 1 kΩ for $V < 2$ Volt and 2 kΩ for $V \geq 2$ Volt. The input voltage of port 1, V_1, is integrated and connected to port 2 and the nonlinear resistor current, I_2, is sensed with the CCVS "H" and differentiated and converted into current with the VCCS "G".

SPICE simulations with the macro-model of the memristor are shown in Figs. 9 and 10. In this particular simulation, a monotonically-increasing and piecewise-linear q-φ function is assumed as the memristor characteristic. This function is shown in Fig. 9 (b). The simulated memristor has a value of 1 kΩ when the flux is less than 2 Wb, but it becomes 2 kΩ when the flux is equal or higher than 2 Wb. The critical flux (φ_c) can be varied with the turn-on voltage of the switch in the macro-model. Fig. 9 (a) shows the pinched hysteresis characteristic of the memristor. The input voltage to the memristor is a ramp with a slope of ± 1 V/s. When the input voltage ramps up with a slope of ± 1 V/s, the memristance is 1 kΩ and the slope of the current-voltage characteristics is 1 mA/V before the the flux reaches to the φ_c. But when the flux becomes 2 Wb, the memristance value is changed to 2 kΩ and the slope is now 0.5 mA/V. After the input voltage reaches to the maximum point, it ramps down and the slope is maintained, because the memristance is still 2 kΩ. Fig. 10 shows the memristor characteristics when a step input voltage is applied. Initially the memristance is 1 kΩ, so the input current is 1 mA. When the flux reaches to 2 Wb (1 V $\times$ 2 s), the memristance is 2 kΩ and so the input current is now 0.5 mA as predicted. The developed macro-model can be used to understand and predict the characteristics of a memristor.

† For further detail about the mutator the reader is referred to Chua [1968].

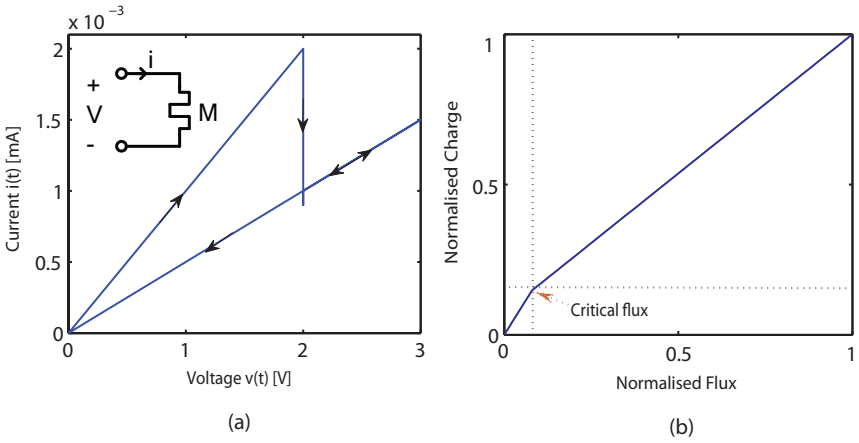

Figure 9. The memristor characteristics. (a) The hysteresis characteristics of the memristor. (b) A monotonically-increasing and piecewise-linear q-φ function as a basic memristor characteristic, the both axes are normalised to their maximum values. The simulated memristor has a value of 1 kΩ when the flux is less than 2 Wb, but it becomes 2 kΩ when the flux is equal or higher than 2 Wb. The critical flux (φ_c) can be varied with the turn-on voltage of the switch in the macro-model. The input voltage to the memristor is a ramp with a slope of ± 1 V/s.

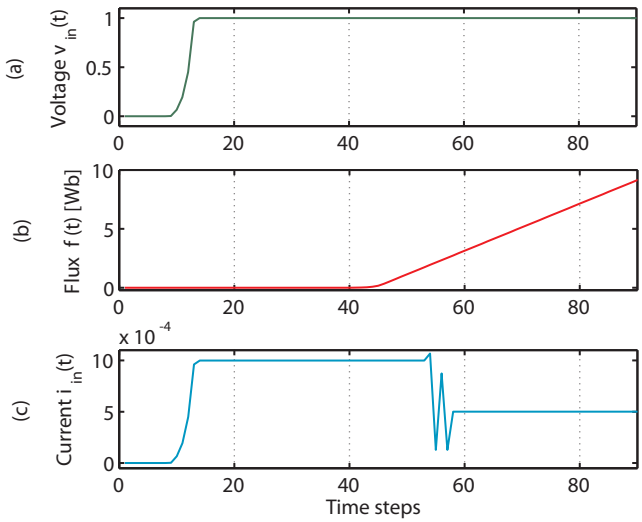

Figure 10. The memristor characteristics when a step input voltage is applied. (a) Voltage curve. (b) Flux linkage curve. (c) Current curve. At the first point the memristance is 1 kΩ, so the input current is 1 mA. When the flux reaches to 2 Wb (1 V $\times$ 2 s, 2 s $=$ 50 time steps), the memristance is 2 kΩ and so the input current is now 0.5 mA as predicted.

Now, if a 1 kHz sinusoidal voltage source is connected across the memristor model, the flux does not reach to 2 Wb so $M = M_1 = 1$ kΩ and $i = 10$ mA. Fig. 11(I) shows the memristor characteristics when a sinusoidal input voltage is applied. As it is shown in Fig. 11(II), when the voltage source frequency reduces to 10 Hz, the flux linkage reaches to 2 Wb within 30 ms. Based on this result, there are two levels of memristance, $M = M_1 =$ 1 kΩ and then it changes to $M_2 = 2$ kΩ.

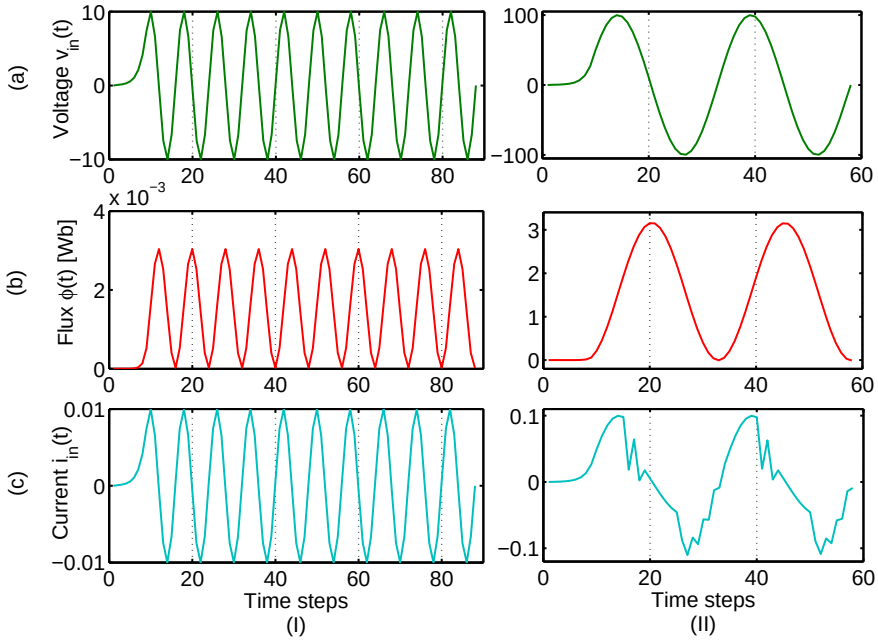

Figure 11. The memristor characteristics when, (I) a 1 kHz sinusoidal voltage is applied. In this case the flux does not reach to 2 Wb so $M = M_1 = 1$ kΩ and $i = 10$ mA. (II) When a 10 Hz sinusoidal voltage is applied. In this case the flux linkage reaches to 2 Wb within 30 ms, or 15 time steps. (a) Voltage curve. (b) Flux linkage curve. (c) Current curve.

Another interesting study is needed to verify that the model is working properly when there is a parallel, series, RM (Resistor-Memristor), LM (Inductor-Memristor), or CM (Capacitor-Memristor) network. First of all, let us assume that there are two memristors with the same characteristic as shown in Fig. 9. Analysing series and parallel configurations of these memristors are demonstrated in Figs. 12(b) and 12(a), respectively. In both figures, the left I-V curve shows a single memristor.

The simulation results show that the series and parallel configurations of memristors are the same as their resistor counterparts. It means the equivalent memristances, M_{eq}, of a two memristor in series and parallel are $M_{\text{eq}} = 2M$ and $M_{\text{eq}} = M/2$, respectively, where M is memristance of a single memristor. The second step is RM, LM, and CM networks. In these cases a 10 V step input voltage has been applied to circuits. As mentioned before for a single memristor based on the proposed model, while the flux linkage is less than or equal to the critical flux, $\varphi \leq \varphi_c$, $M = M_1 = 1$ kΩ and when the flux is more than the critical flux value, $\varphi > \varphi_c$, $M = M_2 = 2$ kΩ. Recall that the critical flux value based on the $q - \varphi$ curve is $\varphi_c = 2$ Wb. Figs. 13(R), 13(C), and 13(L) illustrate RM, CM, and LM circuits and their response to the input step voltage, respectively.

If we assume that the memristance value switches at time T_d, then for $0 \leq t \leq T_d$, $\varphi \leq \varphi_c$, and $M = M_1 = 1$ kΩ. Therefore, in the RM circuit we have, $V_M = V\frac{M_1}{R+M_1}$. For $R = 1$ kΩ, $V_M = 5$ V and then $i_M = 5$ mA, so $T_d = \frac{\varphi_c}{V_M} = 0.4$ s. Likewise, when $t > T_d$, $\varphi > \varphi_c$, we have, $V_M = V\frac{M_2}{R+M_2} = 6.7$ V and $i_M = 3.3$ mA. Both cases have been verified by the simulation results.

In the LM circuit we have the same situation, so for $0 \leq t \leq T_d$, $\varphi \leq \varphi_c$, $V_M = V = 10$ V,

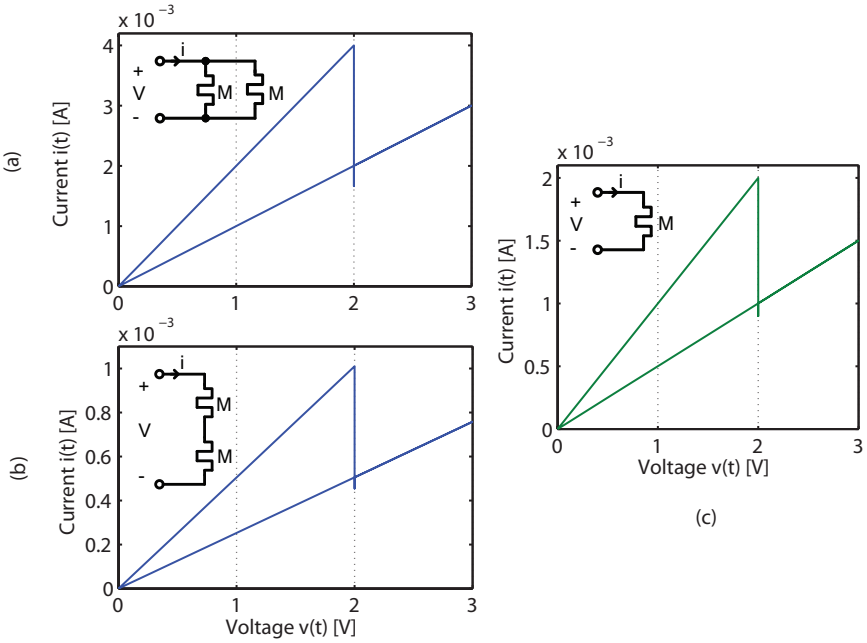

Figure 12. The I-V curves for, (a) two memristors in parallel, (b) two memristor in series, and (c) a single memristor. In all of the cases there is no difference between a memristor and equivalent resistor in the network. In other words, two memristors in parallel, with the same characteristics, form a single memristor with $M_{\rm equ} = M_q/2$ as memristance, and two memristors in series form a single memristor with $M_{\rm equ} = 2M_q$ as memristance.

$i_M = 10$ mA ($R = 1$ kΩ), and $T_d = 0.2$ s. For $t > T_d$, memristor current is $i_M = 5$ mA. Memristor's current changing is clearly shown in Fig. 13(L). The CM circuit simulation also verifies a change in time constant from M_1C to M_2C.

As another circuit example of using the new memristor model, an op-amp integrator has been chosen. The model of an op-amp and circuit configuration is shown in Fig. 14. If $C = 100$ μC then we have 0.1 s and 0.2 s as the time constant of the circuit at $t \leq T_d$ and $t > T_d$, respectively.

It is worth mentioning that, recently, a few simple SPICE macro-models have been proposed by Benderli and Wey [2009], Biolek et al. [2009b] and Zhang et al. [2009] but none of them consider the model response with different circuit elements types, which is an important step to verify the model correctness.

4. Interpreting memristor in Electromagnetic Theory

In his original paper Chua [1971] presented an argumentation based on electromagnetic field theory for the existence of the memristor. His motivation was to interpret the memristor in terms of the so-called *quasi-static expansion* of Maxwell's equations. This expansion is usually used to give an explanation to the elements of circuit theory within the electromagnetic field theory.

Chua's argumentation hints that a memristor might exist, it although never proved that this device can in fact be realised physically. In the following we describe how Chua argued

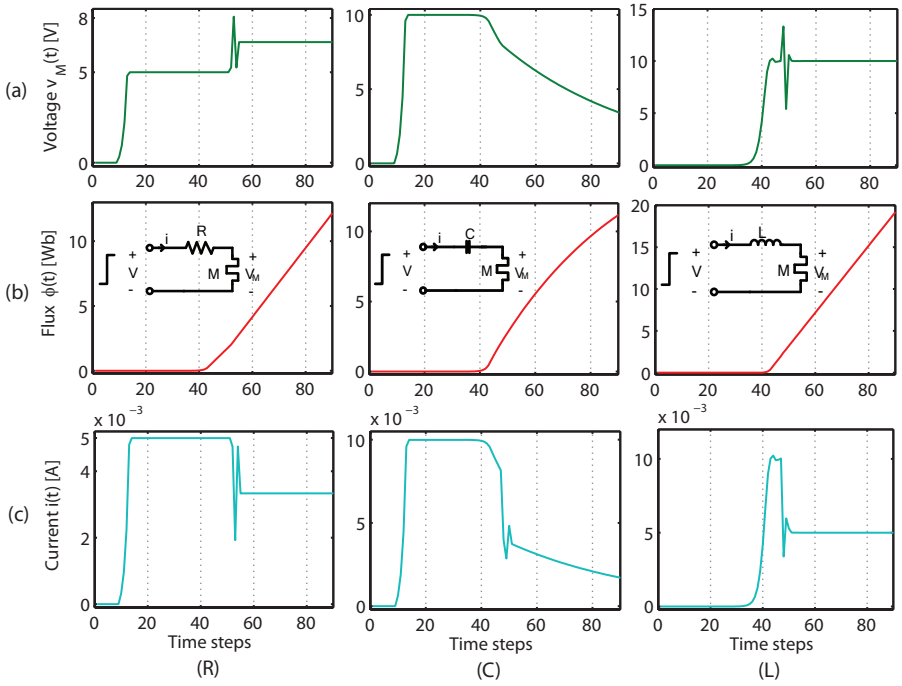

Figure 13. Step voltage response curves for (R) Resistor-Memristor, (C) Capacitor-Memristor, and (L) Inductor-Memristor. (a) Memristor voltage curve, $V_M(t)$. (b) Flux linkage curve, $\varphi(t)$. (c) Current curve, $i_C(t)$. The memristance value switches at time T_d, then for $0 \leq t \leq T_d$, $\varphi \leq \varphi_c$, and $M = M_1 = 1$ kΩ. Therefore, in the RM circuit we have, $V_M = V\frac{M_1}{R+M_1}$. For $R = 1$ kΩ, $V_M = 5$ V and then $i_M = 5$ mA, so $T_d = \frac{\varphi_c}{V_M} = 0.4$ s. Likewise, when $t > T_d$, $\varphi > \varphi_c$, we have, $V_M = V\frac{M_2}{R+M_2} = 6.7$ V and $i_M = 3.3$ mA. In the LM circuit we have the same situation, so for $0 \leq t \leq T_d$, $\varphi \leq \varphi_c$, $V_M = V = 10$ V, $i_M = 10$ mA ($R = 1$ kΩ), and $T_d = 0.2$ s. For $t > T_d$, memristor current is $i_M = 5$ mA.

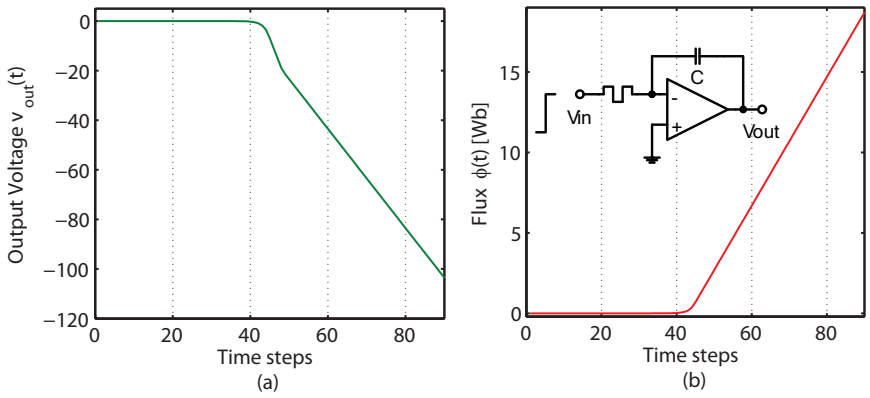

Figure 14. Memristor-op-amp integrator circuit and its response to the input step voltage. (a) Output voltage curve, $V_{\text{out}}(t)$. (b) Flux linkage curve, $\varphi(t)$. If $C = 100$ μC then we have 0.1 s and 0.2 s as the time constant of the circuit at $t \leq T_d$ and $t > T_d$, respectively.

for a memristor from a consideration of quasi-static expansion of Maxwell's equations. To consider this expansion, we use Maxwell's equations in their differential form,

$$\nabla \cdot \mathbf{D} = \rho \ , \tag{4.1}$$

$$\nabla \cdot \mathbf{B} = 0 \ , \tag{4.2}$$

$$\nabla \times \mathbf{E} = -\frac{\partial \mathbf{B}}{\partial t} \ , \tag{4.3}$$

$$\nabla \times \mathbf{H} = \mathbf{J} + \frac{\partial \mathbf{D}}{\partial t} \ , \tag{4.4}$$

where $\mathbf{E}$ is electric field intensity ($\mathrm{V/m}$), $\mathbf{B}$ is magnetic flux density ($\mathrm{Wb/m^2}$), $\mathbf{J}$ is electric current density ($\mathrm{A/m^2}$), ρ is electric charge density ($\mathrm{C/m^3}$), $\mathbf{H}$ and $\mathbf{D}$ are magnetic field intensity ($\mathrm{A/m}$) and electric flux density ($\mathrm{C/m^2}$), $\nabla\cdot$ and $\nabla\times$ are divergence and curl operators.

The idea of a quasi-static expansion involves using a process of successive approximations for time-varying fields. The process allows us to study electric circuits in which time variations of electromagnetic field are slow, which is the case for electric circuits.

Consider an entire family of electromagnetic fields for which the time rate of change is variable. The family of fields can be described by a time-rate parameter α which is time rate of change of charge density ρ. We can express Maxwell's equations in terms of the *family time*, $\tau = \alpha t$, and the time derivative of $\mathbf{B}$ can be written as

$$\frac{\partial \mathbf{B}}{\partial t} = \frac{\partial \mathbf{B}}{\partial \tau}\frac{d\tau}{dt} = \alpha \frac{\partial \mathbf{B}}{\partial \tau}. \tag{4.5}$$

Other time derivatives can be expressed similarly. In terms of the family time, Maxwell's equations take the form

$$\nabla \times \mathbf{E} = -\alpha \frac{\partial \mathbf{B}}{\partial \tau}, \quad \nabla \times \mathbf{H} = \mathbf{J} + \alpha \frac{\partial \mathbf{D}}{\partial \tau}, \tag{4.6}$$

which allow us to consider different values of the family time τ, corresponding to different time scales of excitation. Note that in Eqs. 4.6 $\mathbf{E}$, $\mathbf{H}$, $\mathbf{D}$, $\mathbf{J}$, and $\mathbf{B}$ are also functions of α and τ, along with the position (x,y,z).This allows us [Fano et al., 1960] to express, for example, $\mathbf{E}(x,y,z,\alpha,\tau)$ as power series in α:

$$\mathbf{E}(x,y,z,\alpha,\tau) = \mathbf{E}_0(x,y,z,\tau) + \alpha \mathbf{E}_1(x,y,z,\tau) + \alpha^2 \mathbf{E}_2(x,y,z,\tau) + \ldots, \tag{4.7}$$

where the zero and first orders are

$$\begin{aligned} \mathbf{E}_0(x,y,z,\tau) &= [\mathbf{E}(x,y,z,\alpha,\tau)]_{\alpha=0} = -\nabla \Phi_0, \\ \mathbf{E}_1(x,y,z,\tau) &= \left[\frac{\partial \mathbf{E}(x,y,z,\alpha,\tau)}{\partial \alpha}\right]_{\alpha=0} = -\frac{\partial \mathbf{A}_0}{\partial \tau}. \\ &\ldots \end{aligned} \tag{4.8}$$

Along with these, a similar series of expressions for $\mathbf{B}$, $\mathbf{H}$, $\mathbf{J}$, and $\mathbf{D}$ are obtained and can be inserted into Eqs. 4.6, with the assumption that every term in these series is differentiable with respect to x, y, z, and τ. This assumption permits us to write, for example,

$$\nabla \times \mathbf{E} = \nabla \times \mathbf{E}_0 + \alpha(\nabla \times \mathbf{E}_1) + \alpha^2(\nabla \times \mathbf{E}_2) + ..., \tag{4.9}$$

and, when all terms are collected together on one side, this makes Eqs. 4.6 to take the form of a power series in α that is equated to zero. For example, the first equation in Eq. 4.6 becomes

$$\nabla \times \mathbf{E}_0 + \alpha(\nabla \times \mathbf{E}_1 + \frac{\partial \mathbf{B}_0}{\partial \tau}) + \alpha^2(\nabla \times \mathbf{E}_2 + \frac{\partial \mathbf{B}_1}{\partial \tau}) + ... = 0, \tag{4.10}$$

which must hold for all α. This can be true if the coefficients of all powers of α are separately equal to zero. The same applies to the second equation in Eqs. 4.6 and one then obtains the so-called *n* th-order Maxwell's equations, where $n = 0, 1, 2, ...$ For instance, the *zero-order* Maxwell's equations are

$$\nabla \times \mathbf{E}_0 = 0, \tag{4.11}$$
$$\nabla \times \mathbf{H}_0 = \mathbf{J}_0, \tag{4.12}$$

and the *first-order* Maxwell's equations are

$$\nabla \times \mathbf{E}_1 = -\frac{\partial \mathbf{B}_0}{\partial \tau}, \tag{4.13}$$
$$\nabla \times \mathbf{H}_1 = \mathbf{J}_1 + \frac{\partial \mathbf{D}_0}{\partial \tau}. \tag{4.14}$$

The quasi-static fields are obtained from only the first two terms of the power series Eq. 4.10, while ignoring all the remaining terms and by taking $\alpha = 1$. In this case we can approximate $\mathbf{E} \approx \mathbf{E}_0 + \mathbf{E}_1$, $\mathbf{D} \approx \mathbf{D}_0 + \mathbf{D}_1$, $\mathbf{H} \approx \mathbf{H}_0 + \mathbf{H}_1$, $\mathbf{B} \approx \mathbf{B}_0 + \mathbf{B}_1$, and $\mathbf{J} \approx \mathbf{J}_0 + \mathbf{J}_1$.

Circuit theory, along with many other electromagnetic systems, can be explained by the zero-order and first-order Maxwell's equations for which one obtains *quasi-static fields* as the solutions. The three classical circuit elements *resistor*, *inductor*, and *capacitor* can then be explained as electromagnetic systems whose quasi-static solutions correspond to certain combinations of the zero-order and the first-order solutions of Eqs. 4.11-4.14.

However, in this quasi-static explanation of circuit elements, an interesting possibility was unfortunately dismissed [Fano et al., 1960] as it was thought not to have any correspondence with an imaginable situation in circuit theory. This is the case when both the first-order electric and the first-order magnetic fields are *not* negligible. Chua argued that it is precisely this possibility that provides a hint towards the existence a fourth basic circuit device.

Chua's argumentation goes as follows. Assume there exists a two-terminal device in which $\mathbf{D}_1$ is related to $\mathbf{B}_1$, where these quantities are evaluated instantaneously. If this is the case then this device has the following two properties:

1. Zero-order electric and magnetic fields are negligible when compared to the first-order fields i.e. $\mathbf{E}_0$, $\mathbf{D}_0$, $\mathbf{B}_0$, and $\mathbf{J}_0$ can be ignored.

2. The device is made from *non-linear* material for which the first-order fields become related.

Assume that the relationships between the first-order fields are expressed as

$$\mathbf{J}_1 = \mathscr{J}(\mathbf{E}_1), \tag{4.15}$$
$$\mathbf{B}_1 = \mathscr{B}(\mathbf{H}_1), \tag{4.16}$$
$$\mathbf{D}_1 = \mathscr{D}(\mathbf{E}_1), \tag{4.17}$$

where $\mathscr{J}$, $\mathscr{B}$, and $\mathscr{D}$ are one-to-one continuous functions defined over space coordinates only. Combining Eq. 4.14, in which we have now $\mathbf{D}_0 \approx 0$, with Eq. 4.15 gives

$$\nabla \times \mathbf{H}_1 = \mathscr{J}(\mathbf{E}_1). \tag{4.18}$$

As the curl operator does not involve time derivatives, and $\mathscr{J}$ is defined over space coordinates, Eq. 4.18 says that the first-order fields $\mathbf{H}_1$ and $\mathbf{E}_1$ are related. This relation can be expressed by assuming a function $\mathscr{F}$ and we can write

$$\mathbf{E}_1 = \mathscr{F}(\mathbf{H}_1). \tag{4.19}$$

Now, Eq. 4.17 can be re-expressed by using Eq. 4.19 as

$$\mathbf{D}_1 = \mathscr{D} \circ \mathscr{F}(\mathbf{H}_1), \tag{4.20}$$

where $\circ$ operator is the composition of two (or more) functions. Also, as $\mathscr{B}$ is a one-to-one continuous function, Eq. 4.16 can be re-expressed as

$$\mathbf{H}_1 = \mathscr{B}^{-1}(\mathbf{B}_1). \tag{4.21}$$

Inserting from Eq. 4.21 into Eq. 4.20 then gives

$$\mathbf{D}_1 = \mathscr{D} \circ \mathscr{F} \circ \left[\mathscr{B}^{-1}(\mathbf{B}_1)\right] \equiv \mathscr{G}(\mathbf{B}_1). \tag{4.22}$$

Eq. 4.22 predicts that an instantaneous relationship can be established between $\mathbf{D}_1$ and $\mathbf{B}_1$ that is realisable in a memristor. This completes Chua's argumentation using Maxwell's equations for a quasi-static representation of the electromagnetic field quantities of a memristor.

5. Conclusion

In this paper, we surveyed key aspects of the memristor as a promising nano-device. We also introduced a behavioural and SPICE macro-model for the memristor and reviewed Chua's argumentation for the memristor by performing a quasi-static expansion of Maxwell's equations. The SPICE macro-model has been simulated in PSpice and shows agreement with the actual memristor presented in Strukov et al. [2008]. The model shows expected results in combination with a resistor, capacitor, or inductor. A new op-amp based memristor is also presented and tested.

Nanoelectronics not only deals with the nanometer scale, materials, and devices but implies a revolutionary change even in computing algorithms. The Von-Neumann architecture is the base architecture of all current computer systems. This architecture will need revision for carrying out computation with nano-devices and materials. There are many of different components, such as processors, memories, drivers, actuators and so on, but

they are poor at mimicking the human brain. Therefore, for the next generation of computing, choosing a suitable architecture is the first step and requires deep understanding of relevant nano-device capabilities. Obviously, different capabilities might create many opportunities as well as challenges. At present, industry has pushed nanoelectronics research for highest possible compatibility with current devices and fabrication processes. However, the memristor motivates future work in nanoelectronics and nano-computing based on its capabilities.

In this paper we addressed some possible research gaps in the area of the memristor and demonstrated that further device and circuit modelling are urgently needed. The current approach to device modelling is to introduce a physical circuit model with a number of curve fitting parameters. However, such an approach has the limitation of requiring a large number of parameters. Using a non-linear drift model results in more accurate simulation at the cost of a much more complicated set of mathematical equations. Initially behavioural modelling can be utilised, nonetheless a greater modelling effort is needed to accommodate both the defect and process variation issues. An interesting follow up would be the development of mapping models based on the memristor to neuronmorphic systems that deal with architectural level challenges, such as defect-tolerance and integration into current integrated circuit technologies.

6. Acknowledgements

We would like to thank Leon Chua, at UC Berkeley, for useful discussion and correspondence. This work was partially supported by grant No. R33-2008-000-1040-0 from the World Class University (WCU) project of MEST and KOSEF through CBNU is gratefully acknowledged.

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